Introducing

CoolRunner™-II

RealDigital CPLDs

Ultra Low Power

High Performance

No Compromises

XILINX®

Fast, Efficient Software

CoolRunner-II CPLDs are supported in the latest versions of the Xilinx Integrated Software Environment (ISE) including the free downloadable ISE WebPACK™, the free Web-based WebFITTER™, and ISE Foundation™ — the software package that supports all Xilinx CPLD and FPGA families.

ISE WebPACK

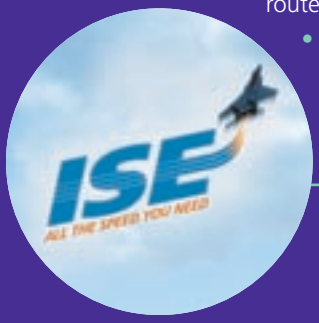
- Free, downloadable, complete pushbutton software solution.
- HDL and ABEL synthesis and simulation.
- JTAG and third-party EDA support.
- Device support for all Xilinx CPLD families (as well as Spartan and Virtex families up to 300K gates).

WebFITTER

- Free Web-based, CPLD design fitting tool.
- Evaluate your designs using CoolRunner-II and all other Xilinx CPLD families.
- Convert existing designs from other CPLD manufacturers into the appropriate Xilinx CPLD.
- Accepts VHDL, Verilog, ABEL, and standard netlists.
- Produces fitting results quickly using the latest versions of Xilinx software.

XPower

- Advanced CPLD and FPGA power estimator.
- Make power estimations early in the system design cycle.
- Analyze total device power, or power per net; for fully routed, partially routed, or un-routed designs.
- Comprehensive GUI-operated tool provides graphic or report-based results.
- Uses your device knowledge and design data to calculate device power.
- Device data is read directly from Xilinx layout files.
- Integrated with ISE Foundation and ISE WebPACK.



Global Services — Finish Faster

Xilinx Global Support increases your productivity and accelerates your time-to-market by providing technical support, localized field application engineers, training, and design services.

Support.xilinx.com (technical support website) — Knowledge at Your Fingertips

- Available 24 hours/day, 7 days/week, 365 days/year.
- Flexible, comprehensive, easy-to-use online resource.
- Includes an Answers Database, discussion groups, interactive problem solvers, software updates, technical tips from Xilinx application engineers, and agents for receiving timely information via email.
- Customize your support.xilinx.com experience with MySupport.

Support Services/Platinum Technical Service — Get to Market Faster

- Premium hotline service with access to senior application engineers, a dedicated toll-free phone number and education credits.

Education Services — Maximize Your Productivity

- Expert, professional instructor-led classes (public or private)
- Eliminate time away from the office through Web-based Live e-Learning

Design Services — Accelerate Your Productivity

- Augment your design team with industry experts in FPGA design techniques and solutions.

CoolRunner™-II

Designing today's advanced systems is a significant challenge.

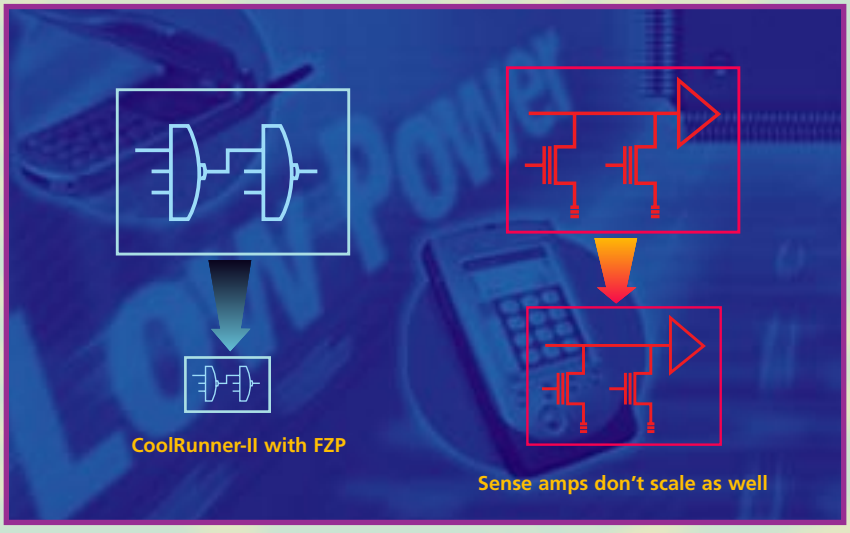
In the past, your only option was to choose a CPLD with either high performance or low power. Now, however, you can get the best of both worlds: high performance and ultra low power in a single device with no compromises.

The new CoolRunner-II CPLD family uses our advanced second generation Fast Zero Power™ (FZP) design technology to give you the best performance with the lowest possible power consumption, and no price premium now or in the future. Featuring a 100% digital core, advanced system features, up to 303 MHz performance, and less than 100 uA of standby current, CoolRunner-II CPLDs are the perfect solution for any new system.

The RealDigital CPLD Advantage

The CoolRunner-II architecture, with its all-digital core, requires far less power than the older CPLD technologies that use power-hungry analog sense amplifiers — with our FZP process technology, there is almost no standby current. Plus, it can be scaled down effectively, beyond it's current 0.18µ geometry, so you can expect even better performance, lower power, and lower costs with future generations — another key advantage over the older technologies that are far more difficult to optimize. Analog CPLDs just can't keep up.

Digital Core vs. Sense Amp



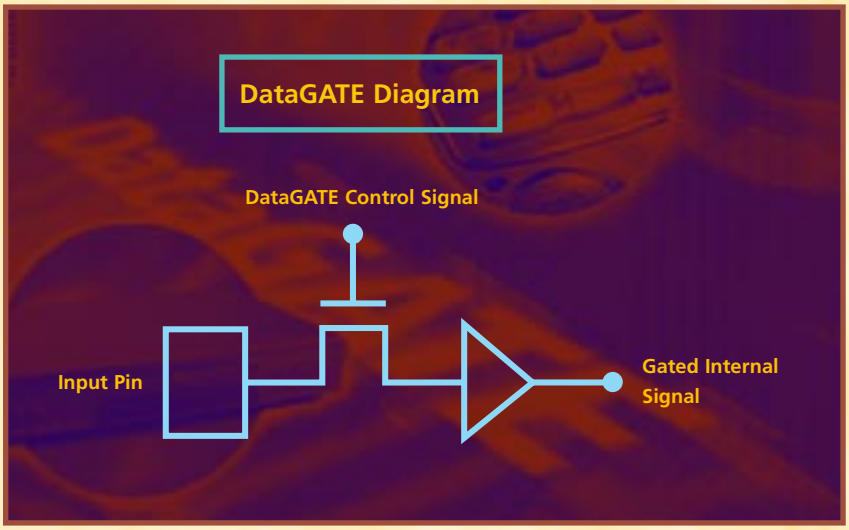
CoolRunner-II Features

The advanced system features in CoolRunner-II devices allow you to integrate many discrete functions, reduce costs, lower power, increase reliability, and decrease your time to market.

Advanced I/O Technology

- Support for multiple I/O standards, including LVTTL, LVCMOS, SSTL, and HSTL. You can easily create standard chip-to-chip and chip-to-memory interfaces and thus remove discrete interface devices from your system. This saves you money and increases your system reliability.
- 400 mV of input hysteresis conditions noisy and slow-rising analog signals.
- DataGATE disables unused input pins, reducing power consumption.

DataGATE

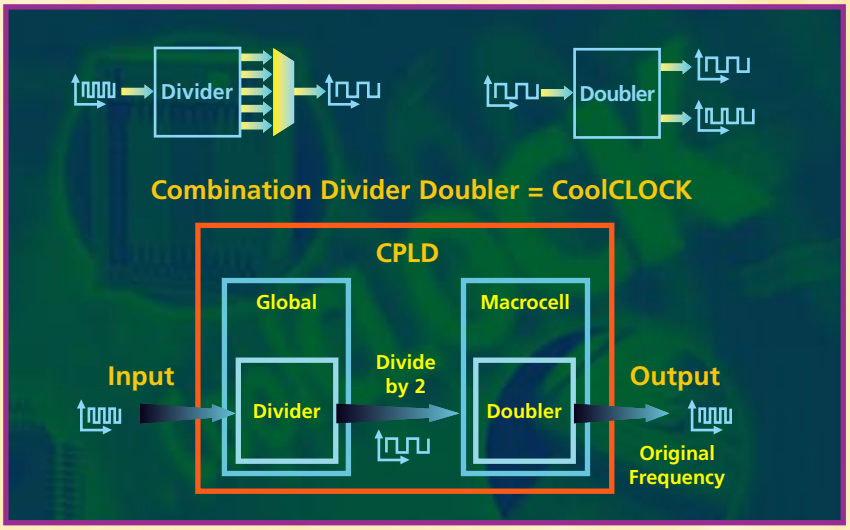


- Bus Hold Output keeps outputs in their last stable state for additional power reduction.
- Up to four independent I/O banks make it easy to use different I/O standards in the same design.

Superior Clock Management

- The Clock Doubler enhances performance by doubling the internal clock speed up to 400MHz. It is selectable for each macrocell and is ideal for Double Data Rate (DDR) memory devices.
- The Clock Divider improves power savings by providing clock division at standard values (2 through 16).
- CoolCLOCK combines the clock divider and doubler; it divides an incoming clock by two (reducing clocking power) and then doubles the clock at the macrocell.

Clock Management



Comprehensive Design Security

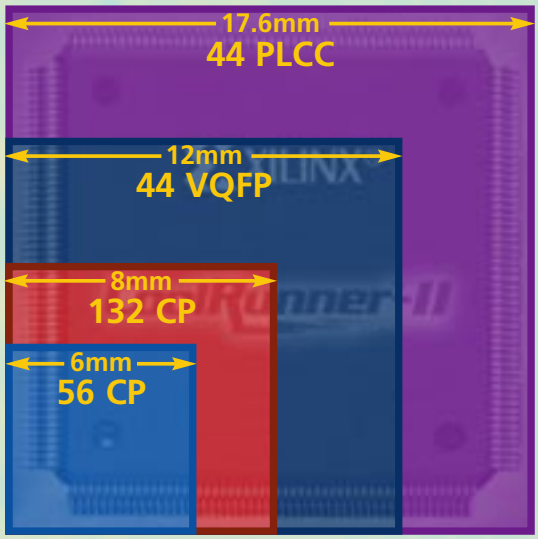
- Designs can be secured during programming to prevent either overwriting or pattern theft via readback.
- Electrical or visual detection of configuration patterns is eliminated with four new levels of on-chip security.
- Electrical or laser tampering causes the device to automatically lock down.
- Protection is buried deeply within the device making it virtually undetectable.

Advanced Packaging

- Small footprint Chip Scale Package (CSP), for space sensitive applications.
- TQFP, PQFP, VQFP, and PLCC packages for cost sensitive applications.
- Fine line BGA packages for high performance applications.

The combination of advanced I/Os, superior clock management, comprehensive security options, and advanced packaging options provides the real world interfaces you need to effectively meet any design challenge.

Small Footprint Packaging Leadership



CoolRunner-II Family at a Glance

	XC2C32	XC2C64	XC2C128	XC2C256	XC2C384	XC2C512
I/O Standards	LVTTL,LVCMOS 15,18,25,33	LVTTL,LVCMOS 15,18,25,33	LVTTL,LVCMOS 15,18,25,33 SSTL 2-1,3-1 HSTL1	LVTTL,LVCMOS 15,18,25,33 SSTL 2-1,3-1 HSTL1	LVTTL,LVCMOS 15,18,25,33 SSTL 2-1,3-1 HSTL1	LVTTL,LVCMOS 15,18,25,33 SSTL 2-1,3-1 HSTL1
Max I/O	33	64	100	184	240	270
T_{PD}(ns)	3.5*	4.0*	4.5*	5.0*	6.0*	6.0*
I/O Banks	1	1	2	2	4	4
Clock double	Yes	Yes	Yes	Yes	Yes	Yes
Input Hysteresis	Yes	Yes	Yes	Yes	Yes	Yes
DataGate & Clock divide			Yes	Yes	Yes	Yes
Packages	VQ44 PC44 CP56	VQ44 PC44 CP56 VQ100	VQ100 CP132 TQ144	VQ100 CP132 TQ144 PQ208 FT256	TQ144 PQ208 FT256 FG324	PQ208 FT256 FG324

* Note: T_{PD} speeds are estimates

Summary

The CoolRunner-II family is the first RealDigital CPLD — a new class of programmable logic devices. Using second generation Fast Zero Power process technology it features a 100% digital core for high performance combined with ultra low power consumption, without a price premium. Now you can get all the benefits of programmable logic for your high performance or portable applications.

For more information, including data sheets, application notes, and reference designs see: **www.xilinx.com/cr2/info**.

Contact your local Xilinx Distributor to learn more.

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