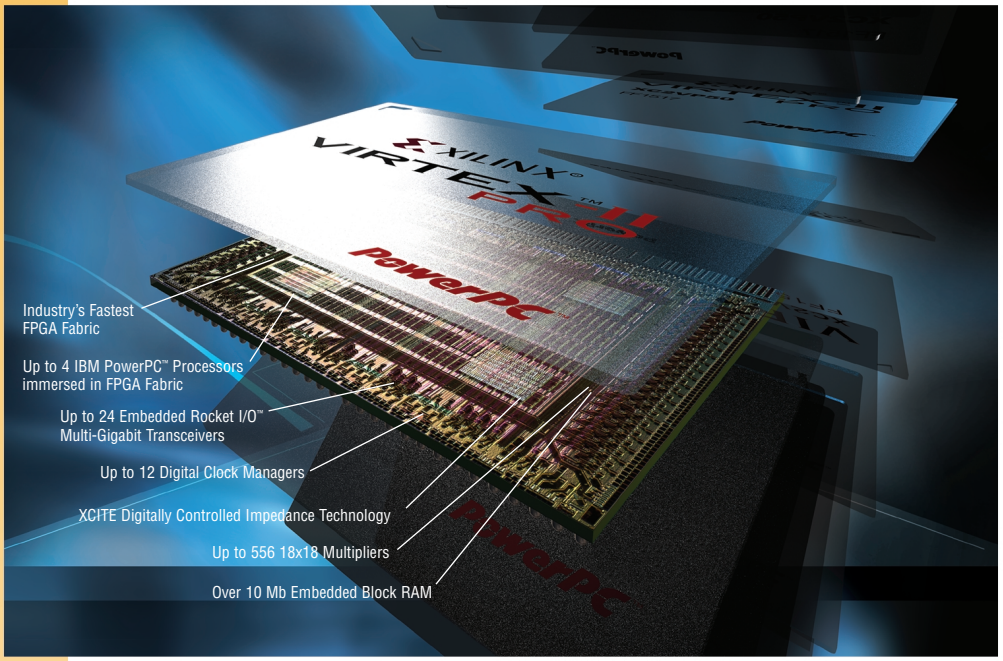
The Platform for Programmable Systems



Developing high-performance systems with embedded processors and fast I/O is quite a challenge. To be successful, you must solve the difficult technical problems of hardware and software development, I/O interfacing, and third-party IP integration; you must rigorously simulate, test, and verify your design; and you must meet increasingly difficult deadlines with a cost-effective product that can adapt as industry standards quickly evolve.

The revolutionary Virtex-II Pro™ family, based on the highly successful Virtex-II architecture, provides a unique platform for developing high-performance microprocessor- and I/O-intensive applications. Virtex-II Pro FPGAs provide up to four embedded 32-bit IBM PowerPC™ RISC processors, each delivering over 420 Dhrystone MIPS at 300 MHz, with a high-bandwidth interface to on-chip programmable logic. In addition, you get up to twenty-four on-chip 3.125 Gbps Rocket I/O™ transceivers to support the emerging connectivity standards such as XAUI, PCI Express (3GIO), and Serial RapidIO. And, because it's programmable, you can easily update your design at any time.

Virtex-II Pro Platform FPGA Family Benefits are Overwhelming

Because all of the critical system components (such as microprocessors, memory, IP peripherals, programmable logic, and high-performance I/O) are located on one programmable logic device, you gain a significant performance and productivity advantage. The Virtex-II Pro FPGA family, along with the Wind River Systems embedded tools and Xilinx ISE development environment, is the fastest, easiest, and most cost effective method for developing your next generation high-performance programmable systems.

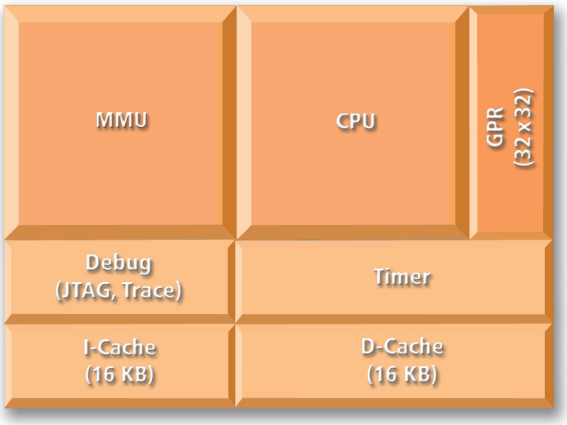
With Virtex-II Pro FPGAs, you get:

- **On-Chip IBM PowerPC Processors** – You get maximum performance and ease of use because these are hard cores, operating at peak efficiency, tightly coupled with all memory and programmable logic resources.
- **The High-Performance Connectivity Solution** – You can implement any of the existing single-ended and differential connectivity standards, such as PCI, HyperTransport, POS PHY, Flexbus, XSBI, and RapidIO, as well as all of the emerging serial connectivity standards such as XAUI, Fibre Channel, Serial ATA, InfiniBand, Serial RapidIO, and PCI Express (3GIO).
- **Excellent Price/Performance Solution** – You can reduce your total bill of material cost and achieve higher performance, while reducing your overall development time. Plus, your product can easily adapt to new requirements, extending its profitability.
- **On-Demand Architectural Synthesis** – You can specify high-level system requirements and generate architecture implementations. The flexibility of the Virtex-II Pro architecture allows you to partition the functionality of the hardware and software at any time during the design and development phase – or even after your product has shipped.
- **Realtime Hardware and Software Debugging** – You can debug your processor software at full hardware speeds while you continue to optimize your hardware design.

Superior Embedded Processing

The Virtex-II Pro processing solution consists of up to four 300+ MHz, 420+ DMIPS IBM PowerPC™ 405 processors, tightly integrated into the FPGA fabric. The IBM PowerPC processor uses a 32-bit Harvard RISC architecture and is extremely popular due to its performance and scalability. The IBM PowerPC processor's key features, coupled with seamless access to surrounding FPGA logic, create a high performance embedded platform. A special on-chip memory interface enables high-speed network applications.

- Up to 300+ MHz Core
- 16KB Data/16KB Instruction Caches
- Memory Management Unit
- Variable page size (1KB-16MB)
- Five-stage datapath pipeline
- Integer multiply/divide unit
- 32 x 32-bit general purpose registers.
- Dedicated on-chip memory interface
- Hardware/software debug and trace
- Multiple processor capability



PowerPC Block Diagram

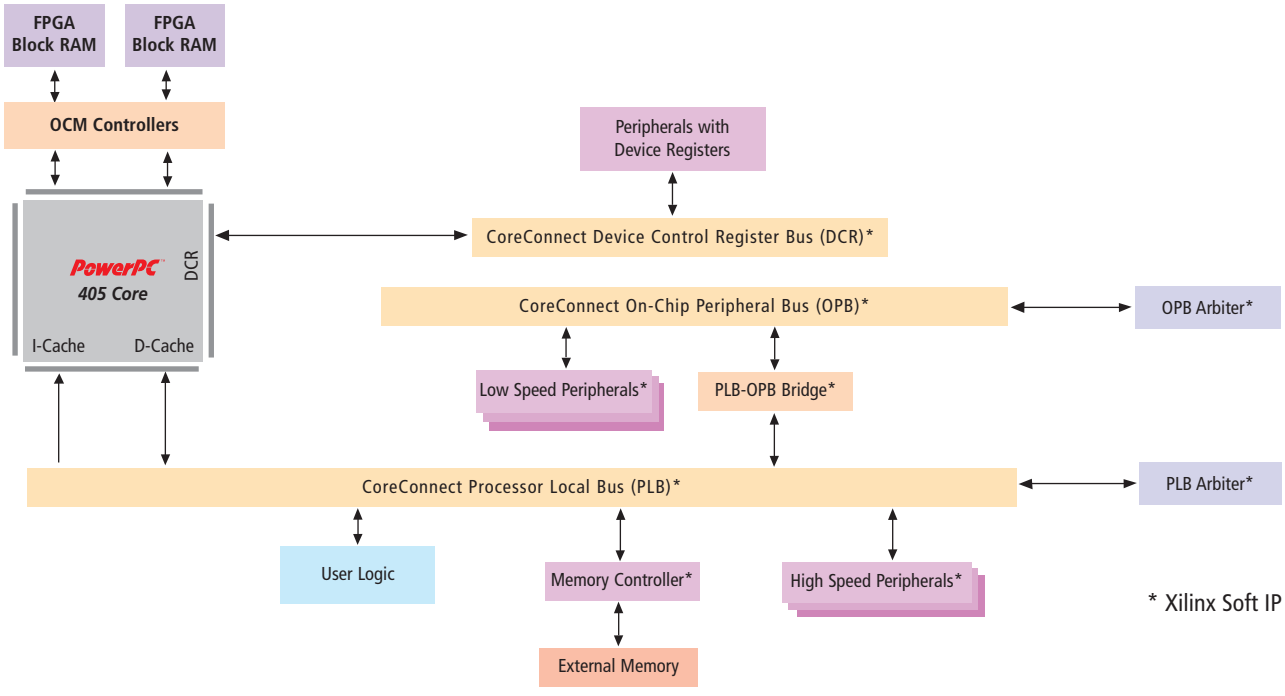
Processor IP and Peripherals

Xilinx offers a wide range of soft IP peripherals, including

- 10/100 Ethernet MAC
- 1 Gb Ethernet MAC
- ATM Utopia L2
- UARTs: 16450, 16550
- Memory Controllers: SDRAM, DDR SDRAM, SRAM, Flash

The IBM CoreConnect™ Bus

The IBM CoreConnect buses – 64 bit Processor Local Bus (PLB), 32 bit On Chip Peripheral Bus (OPB), and 32 bit Device Control Register (DCR) Bus – provide a plug-and-play environment for adding peripherals to the PowerPC processor. Xilinx provides parameterizable peripherals optimized for Virtex-II Pro giving you ultimate flexibility and performance. You can also connect custom peripherals to the bus using the CoreConnect tool kit.



Typical PowerPC System Architecture

The High-Performance Connectivity Solution

Powered by the new Rocket I/O™ serial transceivers, and the proven Xilinx SelectI/O™-Ultra parallel I/O technologies, the Virtex-II Pro family of FPGAs provides the ultimate serial and parallel connectivity platform. Up to twenty-four 3.125 Gbps full duplex Rocket I/O transceivers enable you to achieve an aggregate baud rate of up to 75 Gbps. The SelectI/O-Ultra technology also provides 840 Mbps LVDS, and enables several parallel I/O standards such as LVCMOS, PCI, GTL, HSTL, and SSTL I/O.

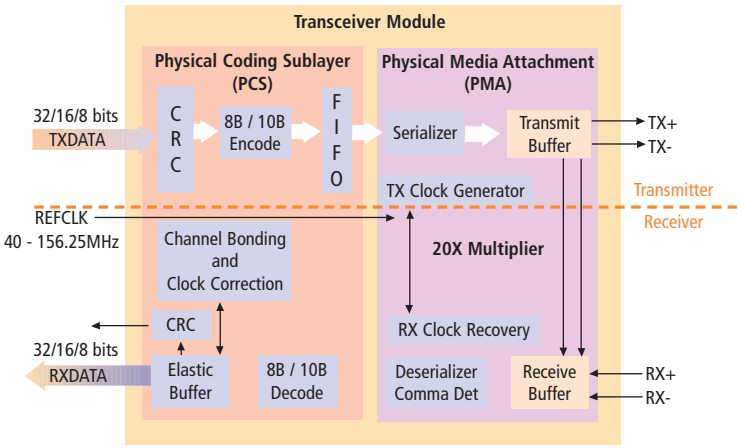
- Full duplex serial transceiver with PCS and PMA modules.
- 622 Mbps to 3.125 Gbps
- 8B/10B encoder/decoder
- Channel bonding
- Scaleable FPGA data path interface
- Monolithic clock synthesis and Clock Data Recovery (CDR)
- Supports 20 inches of FR-4 trace at 3.125 Gbps
- Output swing programmable from 400mV to 800mV

The Leading Price/Performance Solution

The total cost of your design must include not only the various components and PC board space, but also the costs of development, testing, and maintenance; ultimately it must also include the life span of your product and its profitability in the marketplace. Because the Virtex-II Pro family tightly couples all of your key system components onto one, off-the-shelf, programmable device, your design is completed faster and easier, your design performance is not compromised by slower chip-to-chip interconnections, and your product is easier to manufacture and test. Plus, because you can easily make design changes at any time before production — and even after your product is in your customers' hands — your product can more easily adapt to new requirements, and thus stay profitable longer.

Realtime Hardware and Software Debugging

Advanced debugging tools, such as our ChipScope™ Pro, allow you to test both your hardware and your software, at the same time, at full speed, with real-time observability. As a result, you can debug your software while your hardware design is still being refined. You can quickly build a preliminary hardware platform, which lets you start software development much earlier.



Rocket I/O Transceiver Block Diagram

Parallel I/O Standards Supported by Virtex-II Pro SelectI/O-Ultra Technology

Parallel Standard *(Single ended/Differential)*	Interface	Max Data Rate per channel
PCI	32 bit, 64 bit, 3.3V PCI	33/66 Mbps
1 Gb Ethernet with GMII	8 bit GMII	125 Mbps
10 Gb Ethernet with XGMII	32 bit HSTL	312.5 Mbps
RapidIO	8/16 bit LVDS	500 Mbps
POS PHY Level 3	32 bit CMOS	104 Mbps
POS PHY Level 4	16-bit LVDS	840 Mbps
Flexbus 4	64-bit HSTL	200 Mbps
HyperTransport	2/4/8/16/32 bit HyperTransport (LDT)	800 Mbps
CSIX	32 bit HSTL	200 Mbps
XSBI	16-bit LVDS	644 Mbps
SFI-4	16-bit LVDS	622 Mbps

Serial I/O Standards S upported by Virtex-II Pro Rocket I/O Technology

Serial Standard	Data Rate Per Channel	Baud Rate Per Channel
InfiniBand	2.0 Gbps	2.5 Gbps
1 Gb Ethernet 1000BASE-CX/SX/LX	1.0 Gbps	1.25 Gbps
10 Gb Ethernet (XAUI)	2.5 Gbps	3.125 Gbps
Fibre Channel	0.85/1.7 Gbps	1.06/2.12 Gbps
Serial ATA	1.2 Gbps	1.5 Gbps
Serial RapidIO	2.5 Gbps	3.125 Gbps
PCI Express (3GIO)	2.0 Gbps	2.5 Gbps

On-Demand Architectural Synthesis

Architectural synthesis, an extension of behavioral synthesis, is a combination of tools and technologies that generates new system architectures and partitions between hardware and software, based on your high-level requirements. Just as behavioral synthesis enables hardware design by specifying high-level parameters, architectural synthesis enables system-level synthesis, and thus reduces your development time and minimizes your risk.

The Virtex-II Pro family, with its combination of IBM PowerPC cores, abundant memory, high-performance logic, and high speed I/O, provides a platform to easily and optimally partition your hardware and software, at any time.

And Much More...

There is no faster, easier, or more cost-effective method for developing high-performance systems. Visit our website or call your local Xilinx sales representative for the full details, including data sheets and application notes.

For the latest information on the Virtex-II Pro family of FPGAs go to
www.xilinx.com/virtex2pro

The Virtex-II Pro Family

Device	2VP2	2VP4	2VP7	2VP20	2VP30	2VP40	2VP50	2VP70	2VP100	2VP125
Logic Cells	3,168	6,768	11,088	20,880	30,816	43,632	53,136	74,448	99,216	125,136
Block RAM (Kbits)	216	504	792	1,584	2,448	3,456	4,176	5,904	7,992	10,008
18 x18 Multipliers	12	28	44	88	136	192	232	328	444	556
Digital Clock Management Blocks	4	4	4	8	8	8	8	8	12	12
Configuration Memory (Mbits)	1.31	3.01	4.49	8.21	11.36	15.56	19.02	25.6	33.65	42.78
IBM PowerPC Processors	0	1	1	2	2	2	2	2	2	4
Rocket I/O Multi-Gigabit Transceivers	4	4	8	8	8	12*	16*	20	20*	24*
Max Available User I/O	204	348	396	564	692	804	852	996	1164	1200
Package										
FG256	140	140								
FG456	156	248	248							
FF672	204	348	396							
FF896			396	556	556					
FF1152				564	692	692	692			
FF1148						804*	812*			
FF1517						804	852	964		
FF1704								996	1040	1040
FF1696									1164*	1200*

*Note: FF1148 and FF1696 packages support higher user I/O and zero Rocket I/O Multi-Gigabit Transceivers

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