XILINX®
The Programmable Logic Company℠

XILINX SPARTAN-3 FPGAs

http://www.xilinx.com/spartan3

Product Selection Matrix

		CLB Resources					Memory Resources			DSP	CLK Resources				I/O Features				Speed		PROM	
		System Gates (see note 1)	CLB Array (Row x Col)	Number of Slices	Logic Cells (see note 2)	CLB Flip-Flops	Max. Distributed RAM Bits	# Block RAM	Block RAM (kbits)	Dedicated Multipliers	DCM Frequency (min/max)	# DCMs	Frequecny Synthesis	Phase Shift	Digitally Controlled Impedance	Number of Differential I/O Pairs	Maximum I/O	I/O Standards	Commercial Speed Grades (slowest to fastest)	Industrial Speed Grades (slowest to fastest)	Platform Flash PROM	Configuration Memory (Bits)
	Spartan-3 Family – 1.2 Volt																					
SPARTAN-3	**XC3S50**	50K	16 x 12	768	1,728	1,536	12K	4	72K	4	25/326	2	YES	YES	YES	56	124	Single-ended LVTTL, LVCMOS3.3/2.5/1.8/ 1.5/1.2, PCI 3.3V – 32/64-bit 33MHz, SSTL2 Class I & II, SSTL18 Class I, HSTL Class I, III, HSTL1.8 Class I, II & III, GTL, GTL+ Differential LVDS2.5, Bus LVDS2.5, Ultra LVDS2.5, LVDS_ext2.5, RSDS, LDT2.5	-4 -5	-4	XCF01S	.4M
	XC3S200	200K	24 x 20	1,920	4,320	3,840	30K	12	216K	12	25/326	4	YES	YES	YES	76	173		-4 -5	-4	XCF01S	1.0M
	XC3S400	400K	32 x 28	3,584	8,064	7,168	56K	16	288K	16	25/326	4	YES	YES	YES	116	264		-4 -5	-4	XCF02S	1.7M
	XC3S1000	1000K	48 x 40	7,680	17,280	15,360	120K	24	432K	24	25/326	4	YES	YES	YES	175	391		-4 -5	-4	XCF04S	3.2M
	XC3S1500	1500K	64 x 52	13,312	29,952	26,624	208K	32	576K	32	25/326	4	YES	YES	YES	221	487		-4 -5	-4	XCF08P	5.2M
	XC3S2000	2000K	80 x 64	20,480	46,080	40,960	320K	40	720K	40	25/326	4	YES	YES	YES	270	565		-4 -5	-4	XCF08P	7.7M
	XC3S4000	4000K	96 x 72	27,648	62,208	55,296	432K	96	1,728K	96	25/326	4	YES	YES	YES	312	712		-4 -5	-4	XCF16P	11.3M
	XC3S5000	5000K	104 x 80	33,280	74,480	66,560	520K	104	1,872K	104	25/326	4	YES	YES	YES	344	784		-4 -5	-4	XCF16P	13.3M

Note: 1. System Gates include 20-30% of CLBs used as RAMs
2. Logic cell is defined as a 4 input LUT + Flip-Flop + Carry Logic

Verify all data in this document with the device data sheet at http://www.xilinx.com/spartan3

Package Options and User I/O

		Spartan-3								
			XC3S50	XC3S200	XC3S400	XC3S1000	XC3S1500	XC3S2000	XC3S4000	XC3S5000
Pins	**Body Size**	**I/O's**	**124**	**173**	**264**	**391**	**487**	**565**	**712**	**784**
VQFP Packages (VQ) – very thin TQFP (0.5 mm lead spacing)										
100	14 x 14 mm		63	63						
TQFP Packages (TQ) – thin QFP (0.5 mm lead spacing)										
144	20 x 20 mm		97	97	97					
PQFP Packages (PQ) – wire-bond plastic QFP (0.5 mm lead spacing)										
208	28 x 28 mm		124	141	141					
FGA Packages (FT) – wire-bond thin BGA (1.0 mm ball spacing)										
256	17 x 17 mm			173	173	173				
FGA Packages (FG) – wire-bond fine-pitch BGA (1.0 mm ball spacing)										
456	23 x 23 mm				264	333	333			
676	27 x 27 mm					391	487	489		
900	31 x 31 mm							565	633	633
1156	35 x 35 mm								712	784

Note: Numbers indicated in the Package Options and User I/O matrix indicate the maximum number of user I/Os for that package and device combination.