XAPP077 January, 1997 (Version 1.0) Application Note

Summary

Metastability is unavoidable in asynchronous systems. However, using the formulas and test measurements supplied here, designers can calculate the probability of failure. Design techniques for minimizing metastability are also provided.

Xilinx Families

XC7300, XC9500

Introduction

Metastability in digital systems can occur when the data input to a flip-flop is asynchronous to the clock, which can lead to setup or hold time violations. Metastability can appear as a flip-flop that switches late or doesn't switch at all. It can present a brief pulse at a flip-flop output (called a runt pulse) or cause flip-flop output oscillations. Any of these conditions can cause system failures.

The usual cause of metastability is a setup time violation, as demonstrated in Figure 1. If setup time violation is unavoidable, it is possible to calculate how frequently the flip-flop will fail. The industry standard formula for Mean Time Between Failures (MTBF) for a metastable flip-flop is given by:

$$MTBF = (e^{(-C2*tMET)}) / (C1*Fc*Fd)$$

where:

- e = 2.718281828...
- t_{MET} = time delay for the metastability to resolve itself
- F_C = the clocking frequency
- Fd = the data frequency
- C1 = a constant representing the metastability catching setup time window
- C2 = a constant describing the speed with which the metastable condition is resolved

This formula has been used over the last 25 years and is found to be accurate. The variables in the expression are functions of the flip-flop design, its process technology, the clocking rate, and the data switching speed, which are discussed in the following sections.

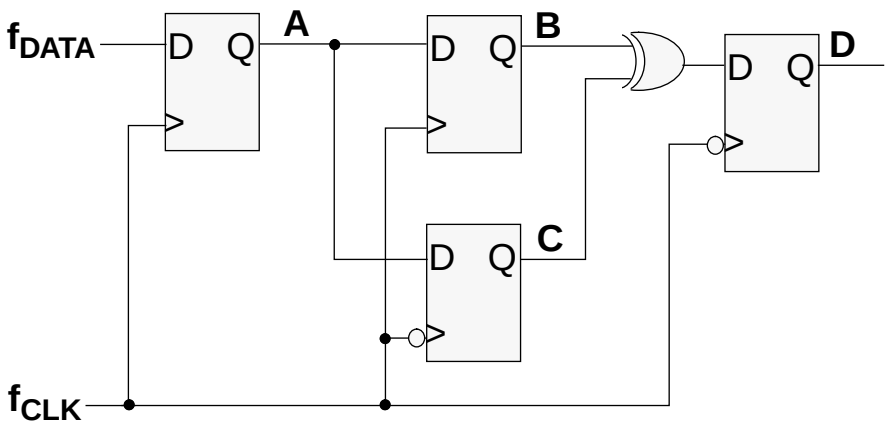

Figure 1: Metastability Measurement Circuit

Metastability Measurement

To test for metastability, a flip-flop is isolated within the CPLD and a clock is applied with asynchronous data input. The data is applied by an independent clocking source that is not related to the signal attached to the flip-flop clock input. The flip-flop eventually encounters a metastable state, which is observed by comparing the state of the flip-flop with it's state at a subsequent time, before the state should have changed again. If the state samples do not match, a metastable condition has occurred and a counter is incremented.

Two other questions must also be answered, and are given time parameters corresponding to their longevity:

- How often does metastability occur (related to C1)?
- How long does the metastable state persist when it does occur (related to C2)?

MTBF is inversely proportional to the clock rate (Fc) and the data rate (Fd). In designs having asynchronous data, most designers do not know their data rate, so it is difficult to estimate the MTBF accurately. Usually, a small time period is considered (10 seconds, for example) and the number of clocks and data transitions during the small time is used to define Fc and Fd. As the time delay is increased, the number of failures decreases dramatically.

By counting the number of failures over time, MTBF can be directly calculated. The values are derived by a formula which includes counts of the number of failures and the time delays for sampling.

Metastability Constants for Xilinx CPLDs

As shown in Figure 1, data is applied to flip-flop A asynchronously with respect to the clock input. The output of flip-flop A passes to two other flip-flops and a simple comparison of the two outputs is made. Note that flip-flop C and D are clocked by the inverted clock. If flip-flop B and C are not identical, a logical one will be captured by flip flop D, indicating a metastable event has occurred.

At 25 degrees C, with Vcc = 5.0 volts, several XC7300 and XC9500 devices were repeatedly measured. By knowing two MTBF values and two t_{MET} times, the constants C2 and C1 are obtained through the following expressions:

- $C1 = e^{(-C2 * tMET)} / (MTBF * Fc * Fd)$
- $C2 = Ln (\blacktriangle MTBF) / \blacktriangle t_{MET}$
- Fc = Frequency of the clock (10Mhz for these tests)
- Fd = Frequency of the data (1Mhz for these tests)
- $t_{MET} = (Ln(MTBF * Fc * Fd * C1)) / C2$

For the XC7300 family:

- $C2 = 3.49 * 10^{9}$
- $C1 = 1.0238 * 10^{-15}$

For the XC9500 family

- $C2 = 6.1172 * 10^{9}$
- $C1 = 9.554 * 10^{-18}$

As shown in Figure 2, the MTBF goes up dramatically as additional time delay for sampling the outputs increases. As a point of reference, 1 year is about 31.5 million seconds.

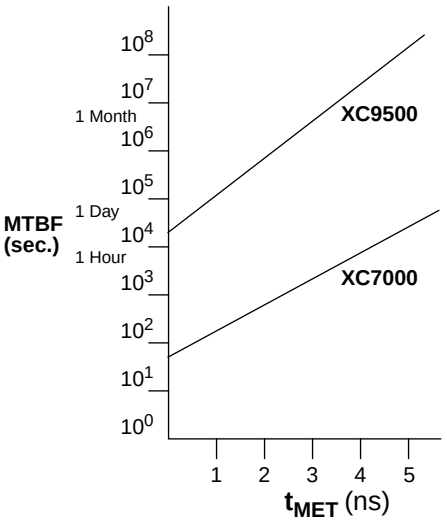

Figure 2: LOG MTBF versus t_{MET}

Design Considerations

To determine how to safely use a flip-flop, using the previous equation:

1. Determine a desired MTBF.
2. Insert the C1 and C2 values into the equation for the chosen flip-flop.
3. Determine whether data transitions are asynchronous or synchronous with respect to the clock. If they are asynchronous, use the average data switching rate calculated in step 4, as follows. If they are synchronous, use the quoted setup and hold times.
4. Calculate t_{MET} using the formula:

   t_{MET} = (Ln(MTBF * Fc *Fd * C1)) / C2

5. If the flip-flop passes through any output that causes it to have delays, add that delay to the t_{MET} expression.

Another way to decrease the effects of metastability is to cascade multiple flip-flops. Because metastability is a statistical effect, the possibility of metastability diminishes for cascaded flip-flops. Figure 3 shows a typical application.

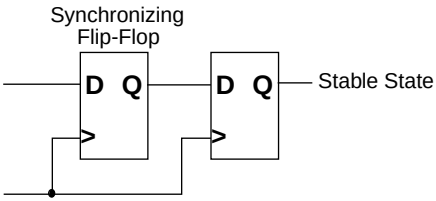

Figure 3: Synchronizing with a Cascaded Flip-Flop

Also, if setup and hold time violations are unavoidable, additional time delay may be added to provide more settling time.

Conclusion

Metastability is unavoidable in asynchronous systems but careful attention to design can usually prevent the problem of violating setup and hold times. Other design techniques exist for improving metastability performance and are described in the following references.

References

1. ANSI/IEEE Std. 1014-1987, IEEE Standard for a Versatile Backplane Bus: VMEbus, Appendix D (Metastability and Synchronization), pg. 281-295
2. Metastable behavior in digital systems, L. Kleeman and A. Cantoni, IEEE Design & Test of Computers, Dec. 1987
3. Measured Flip-Flop Responses to Marginal Triggering. IEEE Transaction on Computers, vol. C-32, no 12, Dec. 1983, pp 1207-1209.
4. High Speed Digital Design (A Handbook of Black Magic), H.W. Johnson and M. Graham, Prentice-Hall, 1993, pp 120 - 131