

Synopsys Introduces *FPGA Express*

New Logic Synthesis Tool Targets Xilinx FPGA Families

Xilinx Alliance member Synopsys unveiled its first entry into the Win95/Windows NT market at the Design Automation Conference in Las Vegas on June 3. "FPGA Express" is a PC-based FPGA



synthesis tool for leading FPGA architectures. The first version has Xilinx XC3000 family, XC4000 series and XC5200 family support. It is scheduled for production shipment in September. Later versions will support the XC9500 CPLD family, as well as other programmable logic vendors.

FPGA Express is unique in its knowledge of Xilinx architectures and tools, allowing designers who are new to HDL to get high-quality results. The expert user will find the sophisticated controls needed to work with very challenging designs.

FPGA Express is not a rewrite of FPGA Compiler, although for compatibility it uses the same VHDL and Verilog compiler technology as Synopsys' workstation tools (Design Compiler and FPGA

Compiler). FPGA Express was designed "from the ground up" with PC users specifically in mind.

The Xilinx/Synopsys relationship was key in the development of this product. "This is an excellent example of Xilinx and one of its Alliance partners working together to meet user requirements with a quality product," noted Wallace Westfeldt, manager of the Xilinx Alliance program.

Xilinx supplied architectural information and assisted in the market research, definition and development of FPGA Express. As a result, FPGA Express makes optimum use of Xilinx device features to maximize density and performance. For example, it includes an automatic module generator that can infer various operations within the HDL source, such as adders, comparators and multipliers, as well as automatically build the circuits using the dedicated carry logic in the XC4000 series and XC5200 family architectures.

FPGA Express also makes full use of complex I/O structures present in the Xilinx devices, including the clock enable feature of the XC4000E IOB registers. Global clock buffers are assigned based on an intelligent algorithm that allocates the available buffers based on clock signal fanout while

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FPGA Express provides a smooth interface to other Xilinx FPGA development tools

filtering out gated clocks. If desired, users can specify specific input pins that need to be connected to a global buffer.

Synopsys revised the mapping and optimization algorithms to provide all HDL users with the best possible synthesis results for area, performance and predictability. Testing has shown that FPGA Express can improve area and performance by up to 25% over existing PC-based synthesis tools. Run times are excellent — a 3,000-gate design compiled in under a minute and a 20,000-gate design required approximately 10 minutes using a Pentium-class computer.

Xilinx also collaborated with Synopsys to integrate FPGA Express into the XACTstep™ system. FPGA Express uses a sophisticated constraint-entry GUI, with an “XACTstep-like” from/to syntax for timing

constraints that directly translates to the XACTstep TIMESPEC format. All netlist and constraint translation is done by FPGA Express, eliminating the need for external translators. The tool outputs Unified Library XNF with group TIMESPECS. The result is a “plug & play” interface between FPGA Express and the XACTstep tools (v6.0.x and beyond).

Pricing and Availability

Sold by Synopsys, FPGA Express starts at \$12,000 (one HDL language and support for one FPGA vendor). It will be available in full production in September, running on Windows 95 and Windows NT-based personal computers.

For more information about FPGA Express contact Bruce Jorgens, Product Line Manager for FPGA Products at Synopsys 415-528-4955. ♦

