LogiCORE™

Dual-Channel Serial Distributed Arithmetic FIR Filter

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XILINX®

DSP CORE Generator

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Features

- Input data words from 4 to 16 bits
- Output data words from 2 to 31 bits
- Coefficient width from 4 to 24 bits
- Taps from 3 to 40 for non-symmetric filters
- Support for cascading multiple filters together to create a larger filter
- Full precision
- Scaleable output
- Input and output synchronization signals
- Registered output
- 2's complement input data
- Uses Fast Carry logic for high speed
- High performance and density guaranteed through Relational Placed Macro (RPM) mapping and placement technology

General Description

FIR filters are one of the most basic building blocks used in digital signal processing, taxing the performance that DSP hardware can deliver. Multiply accumulates must be performed at an ever-increasing rate and demands in the billions of MACs per second range are now common.

Field programmable gate arrays (FPGAs) using distributed arithmetic algorithms can implement large numbers of taps at MHz data sample rates, outperforming DSP processors by one or two orders of magnitude. Sample rates can be efficiently handled over a wide range by applying the proper structure that just meets the required performance with the least number of FPGA configurable logic blocks (CLBs).

Serial distributed arithmetic operates at relatively slow sample rates (3 to 15 million samples per second) but consumes few CLBs. Bits are processed serially, but all taps are processed in parallel. If higher sample rates are required, structures are available which process 2, 3, 4, or all of the bits in parallel. Multi-rate FIR filters can also be supported, resulting in higher sample rates with the same number of resources.

The dual-channel SDA FIR filter can process two independent channels of data, where both channels have the same set of filter coefficients. The implementation requires no increase in the number of CLBs used as compared to the single SDA FIR filter. The dual-channel SDA FIR filter can only implement non-symmetric filters up to 40 taps.

Functional Description

The FIR filter coefficients are formatted and stored in distributed ROM memory (look-up tables) when the module is generated and full precision is maintained throughout all stages of arithmetic computation. Hand-shake signals are provided to control the flow of data with a bit level clock.

The filter maintains full precision throughout processing. For example, a non-symmetrical 12-bit input data word and 14-bit coefficient would yield a 30-bit result (16-bit LUT + 2 bits adder tree growth + 12-bits data + 1-bit subtracter minus one bit for saturation). The maximum available resolution is automatically calculated by the dual-channel SDA FIR filter dialog box after the balance of the other parameters have been entered and can be displayed by looking at the pull-down menu for Output Data Width. The user can adjust the output to fewer bits if desired. In the above example, the 30-bit number could be scaled to a 12-bit number if desired. Note that this does not significantly reduce the amount of logic required due to the nature of the module design. The important factor is that no noise is introduced into the system as a result of arithmetic operations.

A dual-channel SDA FIR filter processes data in a bit serial fashion, alternately taking data from each channel. This means that to process a data word of length N from a single channel will require N clock cycles. Because two data channels are processed, the module requires 2N clock cycles to process one data word from each channel. This module processes ALL taps of the filter in parallel and therefore requires only 2N clock cycles to process ALL of the filter's taps for each channel. This will influence the frequency of the clock, **C**. The user must supply a clock which is at least 2N times the data sample rate of each channel.

Multiple dual-channel SDA FIR filters can be cascaded together to form a larger filter. See the online User's Guide for more information.

Hand-shake Control

Data must be presented to the two DATA IN buses when the RFD (Ready For Data) output control line is high and before the rising edge of CK (Clock). The ND (New Data) input control line must go high prior to the rising edge of CK, signifying that a new data word is available. ND must not be taken high again until RFD is high or data corruption within the filter may occur.

Valid output data appears on the two RESULT output buses on the same rising clock edge and remains stable until the next rising clock edge. This interval corresponds with the Result Ready output RDY going high.

Pinout

Signal names for the schematic symbol are shown in Figure 1 and described in Table 1.

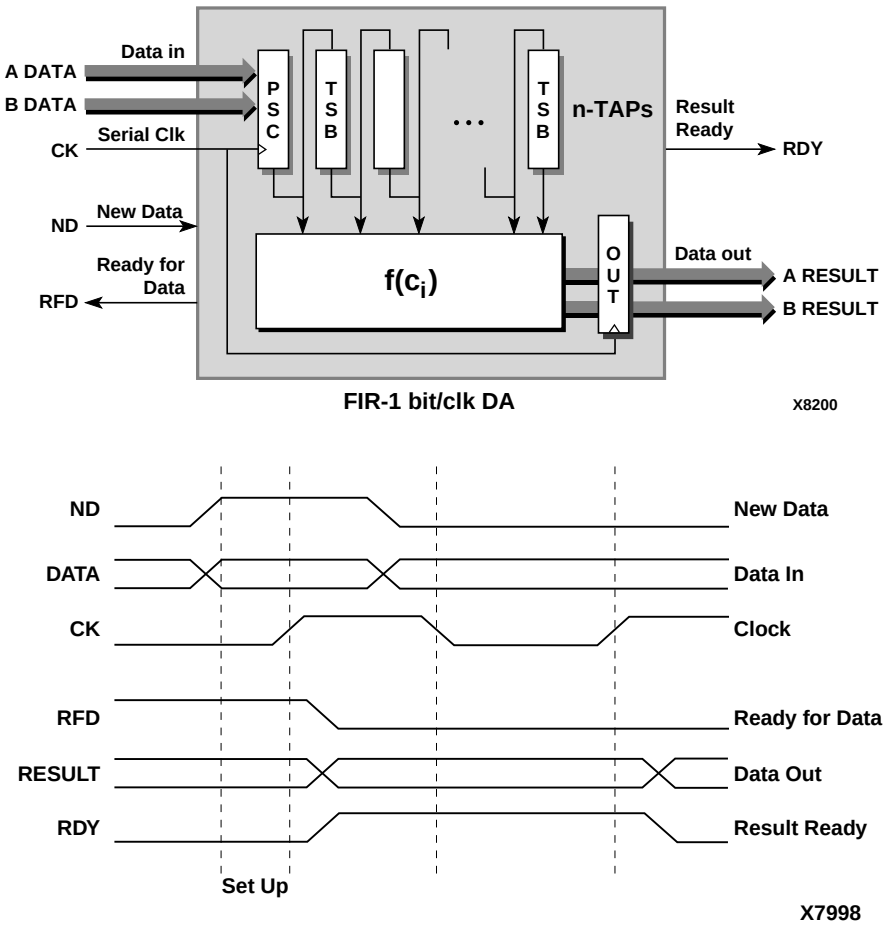

Figure 1. Dual-Channel Serial Distributed Arithmetic FIR Filter Block and Timing Diagrams

Table 1. CORE Signal Pinout

Signal	Signal Direction	Description
A DATA	Input	Channel A Data Input – N-bits wide
B DATA	Input	Channel B Data Input – N-bits wide
CK	Input	Bit rate clock
ND	Input	New Data, active high to indicate that the next rising edge of the clock will cause data to be loaded into the parallel-to-serial converter (PSC).
RFD	Output	Ready For Data – active high when the last data bit is about to leave the PSC and a new data word may be applied and loaded into the filter on the DATA input.
A RESULT	Output	Channel A Data Out – N+x bits wide
B RESULT	Output	Channel B Data Out – N+x bits wide
RDY	Output	Result Ready – active high when the RESULT data is available

Core Generator Parameters

The CORE Generator dialog box for this macro is shown in Figure 2. The parameters are as follows:

- **Component Name**: Enter a name for the component.
- **Input Data Width**: Select an input bit width from the pull-down menu. The valid range is 4-16. If **Reverse Channel B Coefficients** is selected, the valid range is 4-8.
- **Output Data Width**: Full arithmetic precision is carried through the adder trees and scaling accumulator. This parameter selects the number of bits to bring out to the next stage of processing. The valid range is 2-31.
- **Taps:** Select the number of taps from the pull-down menu. The valid range is 3-40.
- **Coefficient Width:** This determines the width of the tables of sums of coefficients. The tables automatically grow from the width specified to accommodate the bit growth as the coefficient sums are calculated. The valid range is 4-24.
- **Trim Empty ROMs:** This option will eliminate the hardware necessary to implement ROM memory if the contents turn out to be all zeros or all ones. This reduces the fanout required, but has the disadvantage of requiring a new filter structure to be generated if the coefficients change.
- **Load Coefficients**: Get the coefficients from a specified file.
- **Show Coefficients**: Display the coefficients after they have been loaded.
- **.coe file**: Displays the name of the coefficient file. This field is read-only.
- **Reverse Channel B Coefficients**: Make Channel B's filter coefficients the reverse of Channel A's. Selecting this option reduces the valid range of the input data width to 4-8.
- **Channel A/B Input Data**: Select Serial or Parallel for both the Channel A and Channel B inputs. When **Reverse Channel B Coefficients** is selected, this field changes to **Channel A Input Data** only. It is useful when cascading multiple filters together to form a larger filter.
- **Channel B Input Data**: Select Serial or Parallel for the input. This field is enabled only when **Reverse Channel B Coefficients** is selected. It is useful when cascading multiple filters together to form a larger filter.

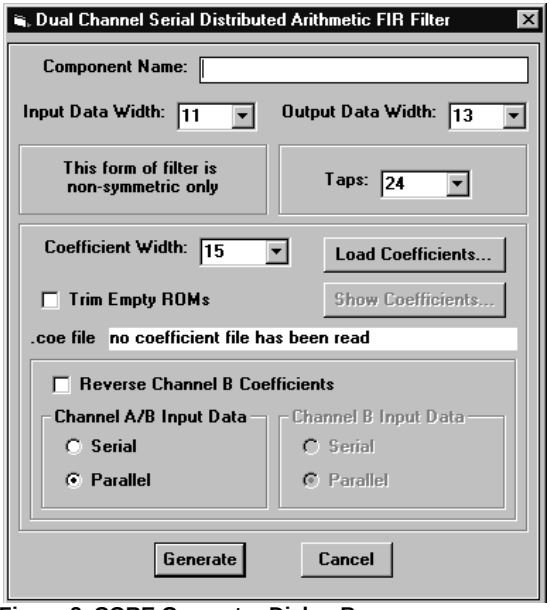

Figure 2. CORE Generator Dialog Box

Core Resource Utilization

Table 2 shows the approximate number of CLBs required for various example bit widths. Table 3 shows the maximum speed for data sample rates using XC4000E-1 devices. The sample rate is calculated by dividing the system clock by the number of bits in the data word (N). Sample rates are independent of the number of taps, but a small increase in delay per clock is a function of the width of the coefficients due to the increase in the width for the adders.

Table 2. CLB Utilization for Example Dual-Channel SDA FIR Filter Implementations

Taps	Symmetry	CLB Counts for Example Data Word Widths[1]						
		8-bit	10-bit	12-bit	14-bit	16-bit	18-bit	20-bit
8	Non-symmetrical	46	54	59	64	69	77	85
16	Non-symmetrical	80	95	104	112	123	138	
24	Non-symmetrical	101	114	127	140	153	174	187

Notes:
1. Coefficient width is equal to the word width.

Table 3. Dual-Channel SDA FIR Filter Data Sample Rates in MHz Using XC4000E-1

Symmetry	5-bit	8-bit	10-bit	12-bit	14-bit	16-bit	18-bit	20-bit
Non-symmetrical	16.0	10.0	8.0	6.7	5.7	5.0	4.4	4.0