SDA FIR Control Logic

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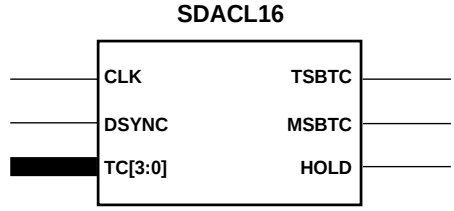

Figure 1: Core Schematic Symbol

Features

- Drop-in modules for the XC4000E, EX, and XL families
- High performance and density guaranteed through Relational Placed Macro (RPM) mapping and placement technology
- Available in Xilinx CORE Generator

Functional Description

This macro accepts a bit serial processing clock input, a data-sync (DSYNC), and a data-width signal (TC) on the input pins to control a Serial Distributed Arithmetic (SDA) process. The DSYNC input is used to start the bit serial process by signaling that a new data sample has arrived for processing. The internal control logic will start counting from 0 to a TC equal to N-2 for N-bit data to produce the outputs TSBTC, MSBTC, and HOLD. The DSYNC input is used to trigger the LSB of the SDA process. TSBTC resets the time-skew buffer and MSBTC disables the macros on the MSB of the SDA process until a new data sample is registered. The process is then repeated.

Pinout

Signal names for the schematic symbol are shown in Figure 1 and described in Table 1.

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
CLK	Input	BIT-PROCESSING CLOCK – clocks the SDA bit serial process. Must have a frequency of N+1 times or greater than the data clock for N-bit data.
DSYNC	Input	DATA SAMPLE READY INPUT – DSYNC is used to reset the Control Logic to begin processing the next data sample. When DSYNC is asserted (HIGH), the input data is registered on the next rising edge of the C (CLOCK). This data is fed into the parallel-to-serial converter and the DSYNC is propagated through the data flow to trigger the LSB input of each cascaded stage of the SDA process. The active duration of DSYNC must be equal to one period, from rising-edge to rising-edge, of the bit processing clock and remain inactive for at least N clock cycles of the bit processing clock for N-bit data.

Table 1: Core Signal Pinout (cont.)

Signal	Signal Direction	Description
HOLD	Output	WAIT UNTIL NEXT SAMPLE – Used to terminate the SDA process. This signal is propagated through the data flow to disable each cascaded stage of the SDA process, as required to maintain data integrity for each clock cycle greater than N+1 for N-bit data.
TC[3:0]	Input	TERMINAL COUNT RESET CONSTANT – Used to terminate the incrementing of the internal counter at TC equal to N-2 for N-bit data.
TSBTC	Output	TIME-SKEW-BUFFER TERMINAL COUNT RESET – Used to reset the TSB Counter at N-1 for N-bit data.
MSBTC	Output	MOST SIGNIFICANT BIT TERMINAL COUNT – Used to indicate the MSB of the SDA process. This signal is propagated through the data flow to trigger the MSB Output of each cascaded stage of the SDA process.

CORE Generator Parameters

The CORE Generator dialog box for this macro is shown in Figure 2. The parameters are as follows:

- **Component Name**: Enter a name for the output files generated for this module.
- **Control Width**: Select a control width from the pull-down menu. The valid range is 2-5. The data width is 2 to this power.

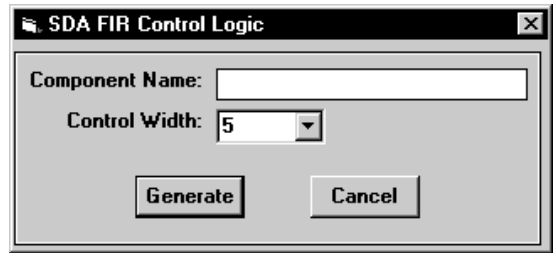

Figure 2: CORE Generator Dialog Box

Core Resource Utilization

An RPM is not generated for this module, so the number of CLBs will vary with the Placer tool.

Ordering Information

This macro comes free with the Xilinx CORE Generator. For additional information contact your local Xilinx sales representative, or e-mail requests to dsp@xilinx.com.