LogiCORE™ Sine/Cosine

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XILINX®

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Features

- Fully parameterizable sin/cos look-up table
- Input address widths from 3 to 10 bits
- Output data widths from 4 to 16 bits
- User can determine the accuracy of the result by selecting the desired output width
- Utilizes fast internal XC4000 distributed ROM
- Easy to use: any table size and output resolution can be specified
- Efficient: calculates full 360 degree table from 90 degree segment
- Useful in high-speed modulation/demodulation applications
- Drop-in modules for the XC4000E, EX, XL, XV and Spartan families
- High performance and density guaranteed through Relational Placed Macro (RPM) mapping and placement technology
- Available in Xilinx CORE Generator

Functional Description

The Sine/Cosine module returns the value **sin(theta)** when the control input (CTRL) is High and the value **cos(theta)** when the control input is Low.

The module contains an internal ROM look-up table that stores only the values for the first quarter of the sine wave. Values of sin(theta) or cos(theta) are derived from this stored data by appropriate negations of the input value and the value fetched from the internal table. The decisions to negate are based on the state of the two most significant bits of theta and the CTRL input.

Support for Signed and Unsigned Theta

The values generated by this module are always expressed in a signed, twos-complement fractional data format. However, values for theta may be provided in either magnitude-only unsigned or twos-complement signed data formats. The format used to express theta has an impact on the precise function performed by the module.

In the case where theta is expressed in an unsigned format, values for theta may range from 0 to 2^{input_width} -1. In the case where theta is expressed in a signed format, values for theta may range from $-2^{(input\_width-1)}$ to $2^{(input\_width-1)}$ -1. In either case, for the purpose of calculating the sine or cosine of theta, the input value is converted to radians as follows:

For signed theta:

$$\theta_{signed} = \frac{2\pi * theta}{2^{(input\_width - 1)}}$$

For unsigned theta:

$$\theta_{unsigned} = \frac{2\pi * theta}{2^{input\_width}}$$

Therefore, the precise function performed by this module, illustrated in the graphics below, is determined by the data format used to express the value theta.

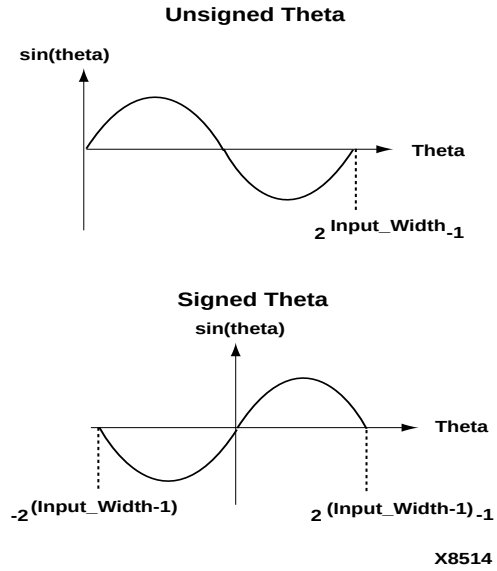

Figure 1: Relationship between Output Function and Input Data Format

Pinout

Port names for the schematic symbol are shown in Figure 2 and described in Table 1.

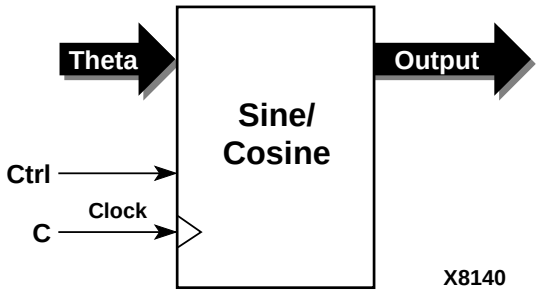

Figure 2: Core Schematic Symbol

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
Theta [n:0]	Input	INPUT VALUE.
Ctrl	Input	CONTROL – when high, returns the sine of theta; when low, returns the cosine.
C	Input	CLOCK - with the exception of asynchronous control inputs (where applicable), control and data inputs are captured, and new output data formed on rising clock transitions.
Output [m:0]	Output	OUTPUT VALUE – the sine or cosine of theta.

Information About Harmonic Content

The sine/cosine values generated by this macro have been carefully calculated and modeled to minimize harmonic content. This results in a signal to noise ratio typically 20dB lower than might be obtained using more traditional parameterizable look-up table methods.

The option to select a greater number of bits in the sine/cosine output obviously reduces the quantization noise (and hence harmonic content) of the waveform. Tables 2 and 3 indicate the 3rd and 5th harmonic content present for a waveform generated by continuous sequential access to this macro, and reflects the lowest possible harmonic content of the fundamental waveform. It is clear that the higher the resolution (output bits) the lower the harmonic content (relative to the fundamental). For a sine/cosine-wave output, all the even harmonics are well below the level of odd harmonics.

The number of points per sine wave generated by the macro can also vary the harmonic content. Naturally the higher the number of points available the better the quality of the sine wave. Normally, a balance is needed when selecting the number of output bits verses the number of points.

The most interesting consequence of reducing the number of points per wave is that higher frequency harmonics can become more pronounced than the nearer harmonics; say, the 3rd and 5th. The levels of some of these notable harmonics are shown in table 4. These values can be alarming until it is realized at which harmonic they occur. They are manifest at a harmonic equivalent to the number of points per wave less one. I.e. a 64 point waveform will have a strong harmonic content at the 63rd harmonic. This is generally of a frequency so far from the fundamental that it's effect is minimal on a system. However, care is required with, say, an 8 point waveform whose 7th harmonic is significant.

Table 2: 3rd Harmonic Content

	1024 pt	512 pt	256 pt	128 pt	64 pt	32 pt	16 pt	8 pt
4 bit	-45	-51	-50	-44	-38	-38	-29	-47
8 bit	-93	-71	-69	-70	-57	-55	-52	-61
12 bit	-116	-98	-94	-82	-83	-76	-77	-81
16 bit	-123	-119	-145	-117	-143	-139	-107	-107

Table 3: 5th Harmonic Content

	1024 pt	512 pt	256 pt	128 pt	64 pt	32 pt	16 pt	8 pt
4 bit	-45	-51	-50	-44	-38	-38	-29	-47
8 bit	-85	-81	-66	-68	-73	-60	-58	-65
12 bit	-96	-98	-94	-104	-96	-100	-98	-82
16 bit	-125	-124	-123	-129	-114	-105	-101	-112

Table 4: Other Harmonics (Harmonic number = Number of points minus 1.)

	1024 pt	512 pt	256 pt	128 pt	64 pt	32 pt	16 pt	8 pt
4 bit	-36	-36	-35	-34	-33	-32	-23	-16
8 bit	-73	-64	-62	-58	-35	-29	-23	-16
12 bit	-93	-86	-85	-84	-35	-29	-23	-16
16 bit	-116	-112	-111	-107	-35	-29	-23	-16

CORE Generator Parameters

The CORE Generator parameterization window for this macro is shown in Figure 2. The parameters are as follows:

- **Component Name**: Enter a name for the component.
- **Input Width**: Select the width of the theta input bus. The valid range is 3 to 10. This value is also used to specify the depth of the required internal look-up table. The number of sample data points in the look-up table is $2^{Input\_Width-2}$
- **Output Width**: Select the width of the look-up table from the pull-down menu. The valid range is 4 to 16. This value determines the precision of the output sin(theta) or cos(theta).

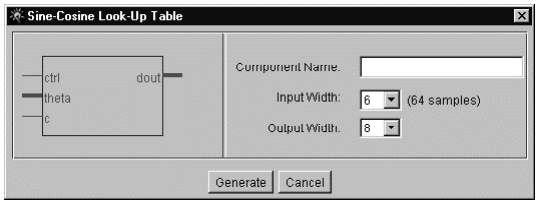

Figure 2: Parameterization Window

Latency

The module has a pipeline latency that depends on the size of the input address width:

Table 4: Latency

Input Width	Latency (# Clocks)
3 to 4 bits	1
5 bits	2
6 to 10 bits	3

Core Resource Utilization

The number of CLBs required for the look-up table depends on the size of the input address width and output data widths selected in the CORE Generator parameterization window.

Table 5 shows the equations to calculate the maximum number of CLBs required for each available input address width. In these equations **m** is the output bit width. (When using these equations, round down to the nearest integer.)

For example, if the input address width is 10 (generating 1024 locations) and the output width is 8 bits, the look-up table requires 74 CLBs.

Table 5: Bit Width versus CLB Count

Input Address Width	CLB Count
3	(m+1)/2
4	m
5	m + (m+1)/2
6	m + 4
7	2m + 4
8	2m + 5 + (m+1)/2
9	4m + 6 + (m+1)/2
10	8m + 6 + (m+1)/2

Ordering Information

This macro comes free with the Xilinx CORE Generator. For additional information contact your local Xilinx sales representative, or e-mail requests to coregen@xilinx.com.

Parameter File Information

Component Name	Type	Notes
Component_Name	String	
Input_Width	Integer	3 -10
Output_Width	Integer	4 -16