LogiCORE™

Non-Symmetric, 32-Deep Time Skew Buffer

March 16, 1998

Product Specification

Xilinx Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
E-mail: coregen@xilinx.com
URL: www.xilinx.com

Features

- Drop-in modules for the XC4000E, EX, XL, XV and Spartan families
- Supports serial word-lengths up to 32 bits
- Uses SelectRAM™ for density and performance
- Handles up to 32 delay stages
- Clock enable for internal registers
- High performance and density guaranteed through Relational Placed Macro (RPM) mapping and placement technology
- Available in Xilinx CORE Generator

Functional Description

This macro accepts a serial data input on the SDI pin. This data is stored in a series of Serially Cascaded, 32-bit Synchronous RAM-based shift registers. Each RAM's output data is registered and presented on the Q pins of the Macro. Each register's Q pin is internally cascaded to the following RAM's Data Input. (See Figure 2, Functional Block Diagram.)The 32-bit RAM-based shift register supports 1- to 32-bit wide data storage per stage. See Figure 2.

The RESET pin is used to control the bit-width of the serial-data to be stored via external control logic.

The internal RAM address is generated internally by a free-running, 5-bit counter (CNT05RE). The counter is controlled by the CE and RESET inputs both active high. See Timing Diagram Figure 3.

Pinout

Port names for the schematic symbol are shown in Figure 1 and Table 2.

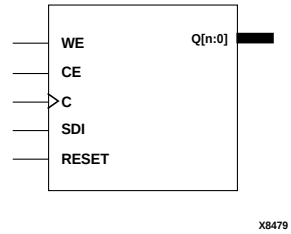


Figure 1: Core Schematic Symbol

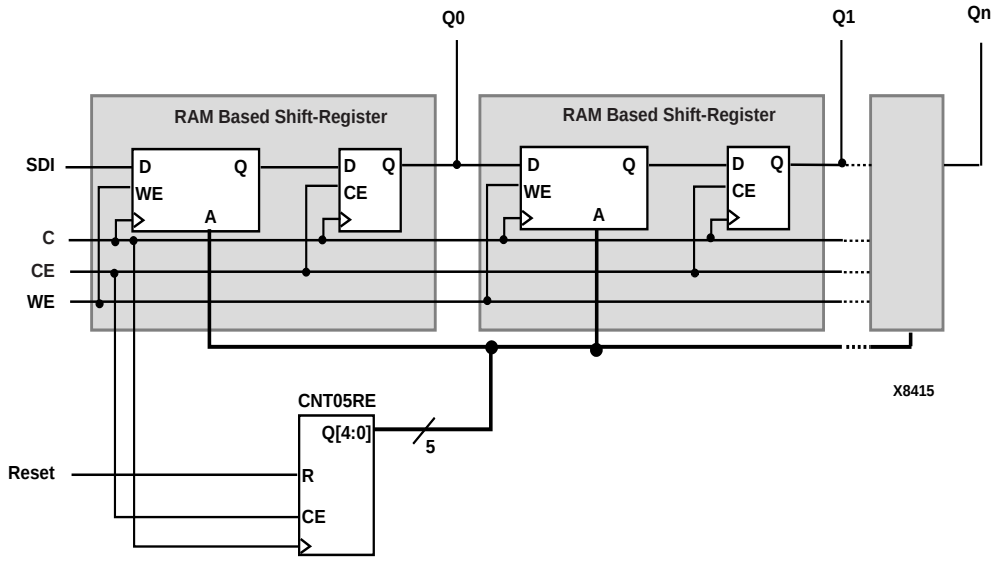


Figure 2: Functional Block Diagram

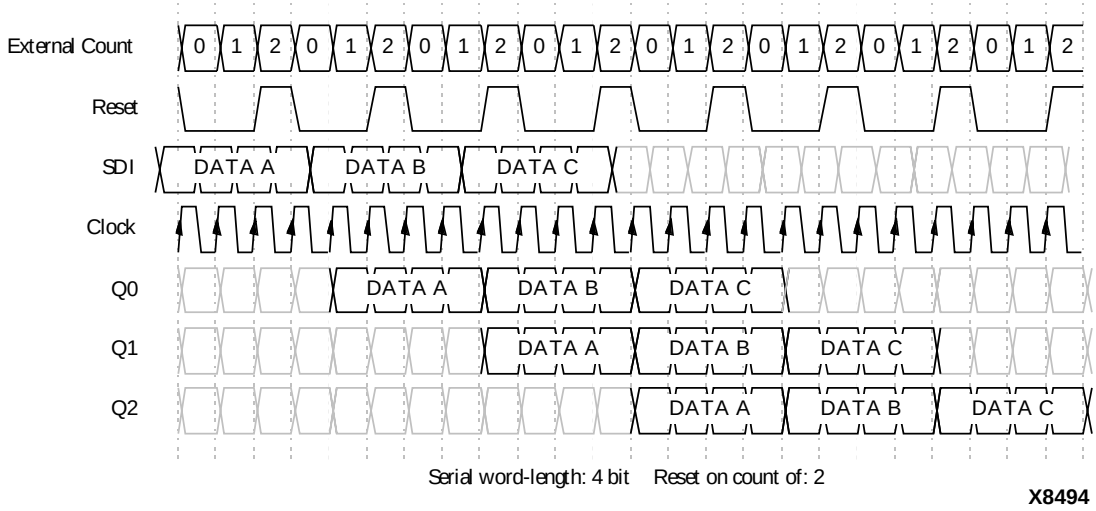


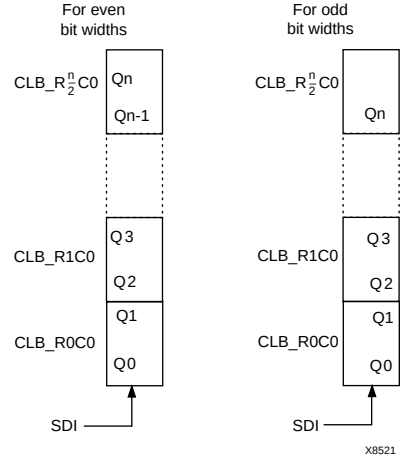
Figure 3: Timing Diagram. Example showing 3 delay stages of 4-bit data.

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
WE	Input	WRITE ENABLE – active high signal, Enables writing to the RAM.
CE	Input	CLOCK ENABLE – active high signal used to allow the transfer of data from the internal RAM to the registered output and the incrementing the Internal Address Counter.
C	Input	CLOCK – clocks the output registers, TSB Counter, and internal synchronous RAM. With the exception of asynchronous control inputs (where applicable), control and data inputs are captured, and new output data formed on rising clock transitions.
SDI	Input	SERIAL DATA INPUT – data presented on this pin is stored into the TSB when the CE (CLOCK ENABLE) and WE (WRITE ENABLE) is asserted (HIGH) and the rising edge of the C (CLOCK).
RESET	Input	TERMINAL COUNT RESET – used to reset the internal RAM's address counter to zero. RESET should be set high at a count of N-2 when string N-bit DATA.
Q[n:0]	Output	REGISTERED OUTPUT DATA – the registered output of the delay stages.

Floorplan Information

This module is functionally identical to the "Non-symmetrical 16-Deep Time Slew Buffer" but differ in terms of its floorplan or layout. This module's floorplan is derived as shown below:



CORE Generator Parameters

The CORE Generator parameterization window for this macro is shown in Figure 2. The parameters are as follows:

- **Component Name**: Enter a name for the output files generated for this module.
- **Output Width**: Select an input bit width from the pull-down menu. The valid range is 2-32.

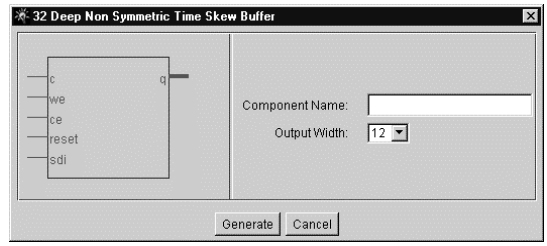


Figure 4: Parameterization Window

Core Resource Utilization

Table 3 shows the number of CLBs required for each available bit width.

Table 3: Bit Width versus CLB Count

Bit Width	CLB Count
2	5
3	6
4	7
5	8
6	9
7	10
8	11
9	12
10	13
11	14
12	15
13	16
14	17
15	18
16	19
17	20
18	21
19	22
20	23
21	24
22	25
23	26
24	27
25	28
26	29
27	30
28	31
29	32
30	33
31	34
32	35

Ordering Information

This macro comes free with the Xilinx CORE Generator. For additional information contact your local Xilinx sales representative, or e-mail requests to coregen@xilinx.com.

Parameter File Information

Parameter Name	Type	Notes
Component_Name	String	
Output_Width	Integer	2 - 32