![Xilinx logo]

FOR IMMEDIATE RELEASE

Ann Duft   Mary Jane Reiter
Xilinx, Inc.   Tsantes & Assoc.
(408) 879-4726   (408) 452-8700
amdennis@aol.com   6526090@mcimail.com

XILINX CARVES LARGER PORTION FROM GATE-ARRAY MARKET WITH INDUSTRY'S FIRST FPGAs UP TO 125,000 GATES

*High–Performance Solution Provides ASIC-like Design Flow
for High–Density FPGA Designs*

SAN JOSE, Calif., January 22, 1996 — Xilinx, Inc. (NASDAQ: XLNX), the world leader in CMOS programmable logic devices, announced today the extension of the industry flagship XC4000E field programmable gate array (FPGA) family to an unprecedented 125,000 usable gates. The new devices, the XC4000EX family, fully exploit the high–density and performance benefits of the XC4000E architecture with additional routing resources, feature enhancements, and support for the popular dual port and synchronous Select–RAM™ feature—the highest performance, most flexible user RAM available. The 100 percent PCI–compliant devices are processed on Xilinx's leading–edge 0.35 micron technology (effective channel length) delivering typical system performance up to 66 MHz.

Complementing the silicon is industry–leading software technology specifically focused at high–density design methodologies leveraging technology obtained from the recent NeoCAD merger; advanced synthesis integration pioneered by Xilinx and its synthesis partners; and new advanced modules recently announced by Xilinx. The

— **more** —
2100 Logic Drive • San Jose, CA 95124-3400
Telephone: 408•559•7778 • FAX: 408•559•7114

combined solution of silicon and software enables users to achieve high density and superior performance with the XC4000EX family.

"Users will be able to create high-density, high-performance designs with the traditional FPGA benefits of reprogrammability and advantage of fast time–to–market, while maintaining their existing design methodologies," said Chuck Fox, vice president, product marketing. "With logic densities ranging from 3,000 to 125,000 usable gates, Xilinx will offer the most powerful solution for the gate array replacement market by addressing 80+ percent of the 1996 ASIC design starts."

On–Chip RAM Functionality and Flexibility through Select–RAM Feature

Like the XC4000E family, each logic block in the XC4000EX devices can be configured as 32 bits of single port or 16 bits of dual port high–speed, synchronous RAM. The distributed RAM implementation allows users ultimate flexibility in selecting the size and location of their RAM functions. The dual port RAM makes the XC4000EX devices ideal for extremely high–speed FIFO designs that are instrumental in delivering single–chip PCI solutions. Using the Select-RAM feature also dramatically increases effective gate counts; for example, in a typical system application using 20 percent of the configurable logic blocks (CLBs) as RAM in a XC40125EX device, the effective "system" gate count rises to 250,000 gates.

"The XC4000EX family allows us to replace high–density ASICs with FPGAs thereby reducing our development risk and providing dramatic savings in ASIC development costs," said Tony Martuscello, senior electrical engineer in the rapid

development group of Lockheed Sanders. "The distributed Select–RAM feature is ideal for building complex DSP functions that previously required a custom ASIC."

Architectural Features Improve Device Performance, Utilization

The major architectural difference between the XC4000E and the XC4000EX devices is the approximate two-fold increase of high–peformance routing resources added to ensure the highest level of device utilization and performance. Xilinx has also patented the redesigned input/output blocks (IOBs) and developed a more flexible, high–speed clock network. The combination delivers four nanosecond setup and six nanoseconds clock–to–out times providing on/off chip delays comparable to gate arrays. New high–speed interconnect, fast IOBs, and advanced process technology enable up to 66 MHz system performance. All XC4000EX devices operate at either five volts or three volts.

High–Performance XACT*step*™ Software

The XC4000EX family will be fully supported in the Xilinx XACT*step* software environment—drawing on new technology from the NeoCAD merger, leading synthesis partnerships, and 11 years of Xilinx engineering.

Among the key technologies obtained from NeoCAD is the FPGA Architect®, a set of architectural capture and evaluation tools, which was used extensively for the development of the XC4000EX devices. It enables rapid software system prototyping and analysis of the routability and performance implications of new architectures. As a result, XC4000EX family users benefit through optimum device utilization and design performance with minimum design iterations and overall design completion times.

Advanced synthesis integration by Xilinx and its synthesis partners includes high–level inference of X-BLOX™ components, architecture specific optimization, and timing constraint interfaces between logic optimization and place/route. These technologies have been extended to support the XC4000EX architecture with added capabilities for Select–RAM implementation.

"Due to our technology partnership with Xilinx, we were involved in the early development cycle to assure seamless compatibility with the new architecture and extend support for the RAM capability. The result is superior design optimization and performance for high–density FPGA designs," says Sanjiv Kaul, director of marketing for Design Implementation Business Unit at Synopsys.

Part of the XC4000EX solution is pre-implemented, fully verified, drop–in modules that allow designers to quickly design in commonly used system–level functions in today's more complex FPGA designs. For example, a PCI–compliant bus interface module will be available to support the XC4000EX family.

Production software will be available on SUN-Sparc, HP-9000, and IBM RS6000 workstations, and PC platforms running Microsoft Windows 95 and Windows NT operating systems by mid-year 1996. Upgrade paths will be available for XACT*step* customers under maintenance contracts.

Pricing for the new devices in the XC4000EX family starts at $695 for the XC4028EX in 100–piece quantities. Volume pricing, in 10,000 unit quantities, is projected to be less than $200 by the end of 1996. HardWire™ gate array versions of the XC4028EX are available for $45 at 25,000 units.

The XC4000EX Family Profile

	Density range		
	Typical	**with RAM**	**Sampling**
Device	**Logic Gates**	**Effective "System" Gates**	**Availability**
XC4028EX	28,000	48,000	Now
XC4036EX	36,000	60,000	2Q96
XC4044EX	44,000	74,000	2H96
XC4052EX	52,000	90,000	2Q96
XC4062EX	62,000	106,000	2H96
XC4085EX	85,000	160,000	1997
XC40125EX	125,000	250,000	1997

Founded in 1984, Xilinx is the world's largest supplier of programmable logic in the semiconductor industry. The company pioneered the market for field programmable gate array (FPGA) semiconductor devices that provide high integration and quick time-to-market for electronic equipment manufacturers in the computer, peripherals, telecommunications, networking, industrial control, instrumentation, and hi-reliability markets. Headquartered in San Jose, Calif., the company produces innovative device architectures and enabling development system software.

— 30 —