An Introduction to Xilinx Products

February 15, 2000

About Xilinx

Xilinx® is the leading provider of complete programmable logic solutions. The company's products help minimize risks for manufacturers of electronic equipment by shortening the time required to develop products and take them to market.

Customers can design and verify their proprietary circuits in Xilinx programmable devices much faster than they could using traditional methods, such as mask-programmed gate arrays. Moreover, because Xilinx devices are standard parts needing only to be programmed, customers are not required to wait for prototypes or pay large non-recurring engineering costs. Customers incorporate Xilinx programmable logic into products for a wide range of markets, including data processing, telecommunications, networking, industrial control, instrumentation, consumer electronics, automotive, military and aerospace.

Founded in 1984, Xilinx pioneered the FPGA, and today fulfills more than half the worldwide demand for field-programmable devices. Xilinx, a publicly traded company (NASDAQ: XLNX) headquartered in San Jose, California, employs approximately 1,800 people worldwide. Market researcher Dataquest currently ranks Xilinx as the seventh-largest ASIC supplier in the world.

Operations

As a "fabless" supplier, Xilinx partners with leading semiconductor manufacturers—UMC Group in Taiwan and Seiko Epson in Japan—through close business relationships or equity positions in their factories. This strategy allows Xilinx to focus on designing new product architectures, software tools and cores while having access to the most advanced semiconductor process technologies. Today Xilinx is producing programmable logic devices using state-of-the-art 0.18- and 0.25-micron process technology, and is working on advanced copper interconnect.

Xilinx has manufacturing operations in San Jose and near Dublin, Ireland, where product design, software development, final testing and quality analysis take place. Xilinx also has facilities in Boulder, Colorado, where much of the company's software development takes place, and in Albuquerque, New Mexico, where development of the CoolRunner CPLDs takes place.

Important Information You Need to Know About This Data Book

Veteran users of Xilinx programmable logic solutions will notice a number of significant changes in this latest edition of the Xilinx Data Book. As always, our goal is to provide you with the most accurate and timely information about Xilinx products.

However, as the world moves at "Internet speed" and the pace of product innovation accelerates, some of the information you see bound between these covers may well have become outdated as the pages were being printed.

The Web Site is Always Current

Whenever Xilinx updates technical data on its products, the first place that information goes is to the Xilinx web site. To find the absolutely latest technical product data from Xilinx, simply go to the following Web address:

www.xilinx.com/partinfo/databook.htm

DataSource CD-ROM

In addition to the challenge of providing you with timely information, there is the problem of sheer bulk associated with printing data books like this one. Over the last few years, Xilinx has introduced a record number of new products, and today Xilinx has the largest product portfolio in the programmable logic industry. As a result, the number of new Xilinx devices and software products continues to grow steadily—to the point that it is impossible to fit complete data sheets on all Xilinx products physically into a single usable volume.

Rather than attempting to publish multiple printed volumes, we have provided the **Xilinx DataSource CD-ROM,** located in the front sleeve of this data book. The CD-ROM contains complete data sheets on all Xilinx products currently in production, as well as all application notes.

Registration Advantage

Please take a moment to compete the registration section on the CD-ROM. This will ensure that you automatically begin to receive quarterly updates of the CD-ROM as they become available. For example, the CD-ROM in this edition of the Xilinx Data Book has an September 2000 expiration date. By registering, you will receive the next updated CD-ROM free of charge and without any other action required on your part.

Data Sheet Categories

In order to provide the most up-to-date information, some component products included in this book may not have been fully characterized at the time of publication. In these cases, the AC and DC characteristics included in the data sheets will be marked as *Advance* or *Preliminary* information. (Not withstanding the definitions of such terms, all specifications are subject to change without notice.) These designations have the following meaning:

- **Advance** — Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or device families. Use as estimates, but not for final production.
- **Preliminary** — Based on preliminary characterization. Changes are possible, but not expected.
- **Final (unmarked)** — Specifications not identified as either Advance or Preliminary are to be considered final.

About This Edition

This data book contains only a snapshot of mainstream Xilinx programmable logic products and brief descriptions and titles of applications note. The data sheets are abbreviated to provide you with basic information on each product line. You can see complete data sheets, pinout tables and application notes either on the current DataSource CD-ROM or by logging on to the data book section of the Xilinx web site. This edition of the data book contains abbreviated descriptions for the following Xilinx product lines:

Virtex™ series FPGAs expand the traditional capabilities of FPGAs to include a powerful set of features that address board level problems for high-performance system designs. The second generation of these devices, the Virtex-E series, is also the industry's first family of FPGAs to offer three million system gates. The Virtex series has numerous built-in features to solve designers' challenges throughout the system: broad capability for chip-to-chip communications through programmable support for the latest I/O standards, digital delay lock loops for clock signal synchronization on the FPGA and on the board, and a memory hierarchy to manage fast access to RAM on and off chip.

Spartan™ series FPGAs are targeted as gate array replacements for low-cost, high-volume designs under 150,000 system gates which require on-chip RAM and can benefit from pre-defined software cores. Spartan devices are optimized for low-cost and are available in 2.5V, 3.3V, and 5V versions. The latest Spartan-II family offers Virtex-like features such as digital delay locked loops, programmable I/O and on-chip block memory.

CoolRunner™ CPLDs are the first to combine very low power with high speed, high density, and high I/O counts in a single device. Xilinx CoolRunner CPLDs feature Fast Zero Power™ technology, allowing them to draw virtually no power in standby mode. CoolRunner CPLDs are ideal for battery operated portable electronic equipment such as laptop PCs, telephone handsets, personal digital assistants and electronic games. These CPLDs also use far less dynamic power during actual operation compared to conventional CPLDs, an important feature for high performance, heat sensitive equipment such as telecom switches, video conferencing systems, simulators, high end testers and emulators. The entire series is available in 3.3V and 5V versions with density ranges beginning at 32 macrocells.

XC9500™ CPLDs from Xilinx range in density from 36 to 288 macrocells and are available in 3.3V and 5V version. XC9500 devices support in-system programming, allowing manufacturers to perform unlimited design iterations during the prototyping phase, extensive system in-board debugging, program and test during manufacturing, and field upgrades. Based on advanced flash memory technology, the XC9500 family provides fast, guaranteed timing, superior pin locking, a full JTAG compliant interface, and 10,000 programming cycles.

QPRO™ Xilinx is the leading supplier of High-Reliability programmable logic devices to the aerospace and defense markets. These devices are used in a wide range of applications such as electronic warfare, missile guidance and targeting, RADAR, SONAR, communications, signal processing, avionics and satellites. The Xilinx QPRO family of ceramic and plastic QML products (Qualified Manufacturers Listing), certified to MIL-PRF-38585, provide system designers with advanced programmable logic solutions for next generation designs. The QPRO family also includes select products that are radiation hardened for use in satellite and other space applications.

The Xilinx QPRO family addresses the issues that are critical to the aerospace and defense market:

QML/Best commercial practices. Commercial manufacturing strengths result in more efficient process flows

Performance-based solutions, including cost-effective plastic packages.

Reliability of supply. Controlled mask sets and processes insure the same quality devices, every time, without variation, which remain in production for an extended time.

Off-the-shelf ASIC solutions. Standard devices readily available, no need for custom logic and gate arrays.

Table of Contents

Products published in this edition of the Xilinx Data Book are listed by page number in the table contents. Product information that is only on the DataSource CD-ROM, such as complete data sheets, application notes and pinout information, is listed as "CD-ROM" in the table of contents.

Xilinx Online

The Xilinx Online program is designed to enable, identify, and promote network upgradable systems. These are systems that can be upgraded, modified, or fixed after they have been deployed in the field. While many customers have been building upgradable devices based on Xilinx technology for years, the explosion of the networked connected devices has dramatically increased the demand for these user configurable and adaptable applications.

Xilinx provides IRL™ technology to make it easier to develop these systems based upon the most advanced programmable logic available. For more information on this program please visit:

www.xilinx.com/xilinxonline

Technical Support

Xilinx provides 24-hour access to a set of sophisticated tools for resolving technical issues via the Web. The Xilinx search utility scans thousands of Answers records to return solutions for the given issue. Several problem-solver tools are also available for assistance in specific areas, like Configuration or Install. A complete suite of one-hour modules is also available at the desktop via live or recorded e-Learning. Lastly, users with a valid service contract can access Xilinx engineers over the Web by opening a case against a specific issue. For technical support on the Web, log on to:

support.xilinx.com

Xilinx is committed to helping users succeed with programmable logic designs and provides a complete and uniquely accessible array of services and training for customers with service contracts. Xilinx experts provide responsive resolutions to problems and creative, timely solutions to design challenges. They also offer design evaluation of new projects and close consultation through the design process. Full training in design completion and methodology review is also available, along with special application consultation.

Internet-enabled Software Solutions

At Xilinx, software tools are a key part of the company's programmable logic solutions. Since its inception, Xilinx has shipped more than 60,000 development systems to customers worldwide. Today Xilinx offers two lines of design and implementation software that are Internet-enabled to allow designers instant and direct access from the tools to the technical support area of the Xilinx web site.

Through its Alliance Series™ software, Xilinx has chosen open systems approach that allows its customers to pick the highest quality and widest variety of design and programming tools available on the market today. To accomplish this, Xilinx has established engineering and marketing relationships with the leading third-party suppliers of electronic design automation (EDA) software. Those include Aldec, Cadence, Data I/O, Exemplar, Mentor Graphics, Model Technology, OrCAD, Synopsys, Synplicity, Veribest and Viewlogic. This open systems strategy extends to front-end design creation, synthesis and verification. The result has been the creation of complementary technology and tightly integrated third-party links with the Xilinx Alliance Series backend place and route software for FPGAs and CPLDs.

Foundation Series™ is a family of a fully integrated, ready-to-use Windows NT and Windows 95 PC tools that support a broad range of FPGA and CPLD design requirements. Available at low price points and targeted at entry-level as well as high end users, the Foundation Series products leverage industry standard hardware description languages (HDLs), including Verilog/VHDL. The Windows-based Foundation Series software provides access to synthesis, schematic entry, gate level simulation and implementation tools. Since Foundation Series tools are integrated into a common design management environment, users have access to all technology from design entry and implementation to verification in a single software package.

WebFitter™ is a unique Internet-based software productivity tool that permits customers anywhere in the world to do on-line fitting of CPLD designs from their PC or workstation. Webfitter kicked off the Xilinx "Silicon Xpresso Initiative" that calls for stepped use of the Internet to help increase designer productivity.

Designers access WebFitter from the Xilinx Web site and work from a graphical user interface integrated with the Netscape browser. WebFitter produces complete on-line reports for design evaluation, and it eliminates the need for designers to load software or manage updates and licenses because the latest Xilinx tools always reside on the Xilinx Web site. WebFitter accepts design files for Xilinx XC9500 and CoolRunner series complex programmable logic devices (CPLDs) and supports VHDL, Verilog, ABEL, XNF or EDIF input formats. After completing a front-end

design, users simply enter their e-mail address, attach their design file and send it to the Xilinx server for compilation. Shortly after, a return e-mail provides a complete fitter report and bitstream to implement the design in the PLD. To get to the WebFitter tool, log on to:

www.xilinx.com/sxpresso/webfitter.htm

The Xilinx WebPACK contains FREE downloadable software solutions for Xilinx XC9500 and CoolRunner Series CPLDs. Each solution provides a simple and intuitive design environment for any Xilinx CPLD family. The WebPACK is a collection of three design suites: design entry, device fitting and programming. These tools can be downloaded and used individually or, when installed together become an integrated design environment for Xilinx CPLDs.

www.xilinx.com/sxpresso/webpack.htm

IP Center Solutions

Today, a large number of predefined cores are available to implement system-level functions directly in Xilinx programmable logic devices. These cores, available from Xilinx and third-party partners, allow designers to cut design time and significantly reduce risk while having access to the best performing and lowest cost components available. Full information about Xilinx cores is available on-line from the IP Center area of the Xilinx Web site. To get to the IP Center, log on to:

www.xilinx.com/ipcenter

LogiCORE™ products are sold and supported directly by Xilinx and include PCI interfaces, digital signal processing (DSP) functions and a number of other modules such as adders, multipliers and look-up tables.

AllianceCORE™ modules are sold and supported by a network of third-party developers and are optimized for Xilinx devices. Current AllianceCORE products range from processors and standard peripheral controllers to ATM functions.

The CORE Generator™ tool from Xilinx delivers highly optimized cores that are compatible with standard design methodologies for Xilinx FPGAs. This easy-to-use tool generates flexible, high performance cores with a high degree of predictability and allows customers to download future core offerings from the Xilinx web site. Both Xilinx and independent IP developers can design cores for the CORE Generator tool, which also serves as a cataloging and delivery system for related collateral for all designers using Xilinx.

Design Consultants

The Xilinx XPERTS Program qualifies, develops and supports design consultants, ensuring that they have superior design skills and the ability to work successfully with customers. XPERTS is a worldwide program that allows easy access to certified experts in Xilinx device architectures, software tools and cores. XPERTS partners also offer consulting in the areas of HDL synthesis and verification, customization and integration, system-level designs and team-based design techniques. A listing of partners in the Xilinx XPERTS program is located on the Web at:

www.xilinx.com/ipcenter

Feedback

We welcome any comments or suggestions you have about the Xilinx Data Book – whether it's the printed, CD-ROM, or web version. You can send your feedback by e-mail to:

Databook@xilinx.com

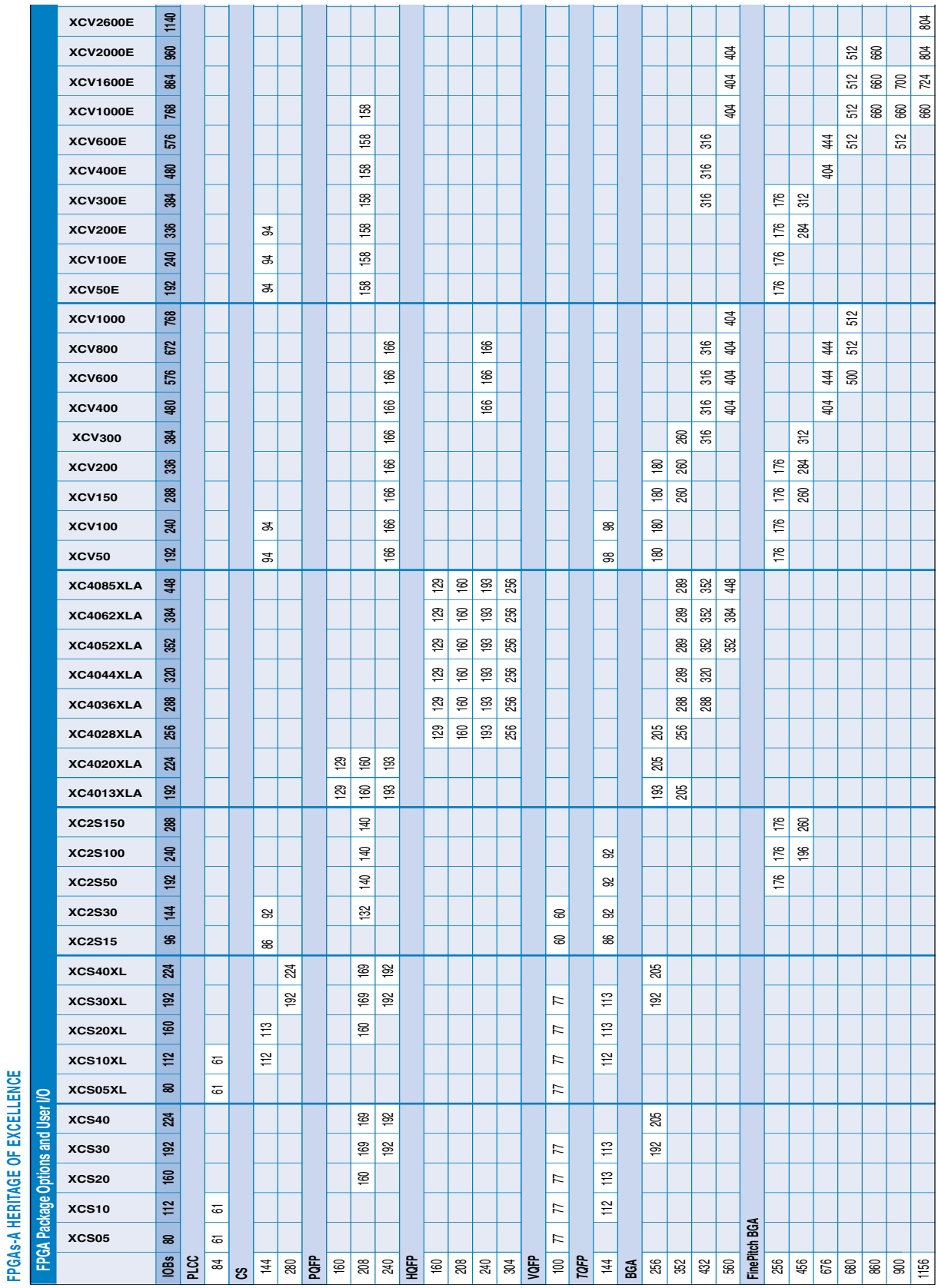

Figure 1: FPGA Package Options and User I/O Selection

FPGA Product Selection Matrix

		DENSITY							FEATURES						
Device	Key Features	Logic Cells	Maximum Logic Gates	Typical System Gate Range	Max. RAM Bits	CLB Matrix	CLBs	Flip-Flops	Max. I/O	Output Drive (mA)	PCI Compliant	1.8 Volt	2.5 Volt	3 Volt	5 Volt
XCS05	Spartan Series: High Volume ASIC Replacement/ High Performance/ SelectRAM Memory	238	3K	2K-5K	3K	10x10	100	360	77	12	Y	–	–	–	X
XCS10		466	5K	3K-10K	6K	14x14	196	616	112	12	Y	–	–	–	X
XCS20		950	10K	7K-20K	13K	20x20	400	1120	160	12	Y	–	–	–	X
XCS30		1368	13K	10K-30K	18K	24x24	576	1536	192	12	Y	–	–	–	X
XCS40		1862	20K	13K-40K	25K	28x28	784	2016	205	12	Y	–	–	–	X
XCS05XL		238	3K	2K-5K	3K	10x10	100	360	77	12/24	Y	–	–	X	*
XCS10XL		466	5K	3K-10K	6K	14x14	196	616	112	12/24	Y	–	–	X	*
XCS20XL		950	10K	7K-20K	13K	20x20	400	1120	160	12/24	Y	–	–	X	*
XCS30XL		1368	13K	10K-30K	18K	24x24	576	1536	192	12/24	Y	–	–	X	*
XCS40XL		1862	20K	13K-40K	25K	28x28	784	2016	224	12/24	Y	–	–	X	*
XC2S15		432	8K	6K-15K	22K	8x12	96	384	86	2/24	Y	–	X	I/O	*
XC2S30		972	17K	13K-30K	36K	12x18	216	863	132	2/24	Y	–	X	I/O	*
XC2S50		1728	30K	23K-50K	56K	16x24	384	1536	176	2/24	Y	–	X	I/O	*
XC2S100		2700	53K	37K-100K	78K	20x30	600	2400	196	2/24	Y	–	X	I/O	*
XC2S150		3888	77K	52K-150K	102K	24x36	864	3456	260	2/24	Y	–	X	I/O	*
XC4013XLA	XC4000 Series: Density Leadership/ High Performance/ SelectRAM Memory	1368	13K	10K-30K	18K	24x24	576	1536	192	12/24	Y	–	–	X	*
XC4020XLA		1862	20K	13K-40K	25K	28x28	784	2016	205	12/24	Y	–	–	X	*
XC4028XLA		2432	28K	18K-50K	33K	32x32	1024	2560	256	12/24	Y	–	–	X	*
XC4036XLA		3078	36K	22K-65K	42K	36x36	1296	3168	288	12/24	Y	–	–	X	*
XC4044XLA		3800	44K	27K-80K	51K	40x40	1600	3840	320	12/24	Y	–	–	X	*
XC4052XLA		4598	52K	33K-100K	62K	44x44	1936	4576	352	12/24	Y	–	–	X	*
XC4062XLA		5472	62K	40K-130K	74K	48x48	2304	5376	384	12/24	Y	–	–	X	*
XC4085XLA		7448	85K	55K-180K	100K	56x56	3136	7168	448	12/24	Y	–	–	X	*
XCV50	Virtex Family: Density/ Performance Leadership BlockRAM Distributed RAM SelectI/O 4 DLLs	1728	21K	34K-58K	56K	16x24	384	1536	180	2/24	Y	–	X	I/O	*
XCV100		2700	32K	72K-109K	78K	20x30	600	2400	180	2/24	Y	–	X	I/O	*
XCV150		3888	47K	93K-165K	102K	24x36	864	3456	260	2/24	Y	–	X	I/O	*
XCV200		5292	64K	146K-237K	130K	28x42	1176	4704	284	2/24	Y	–	X	I/O	*
XCV300		6912	83K	176K-323K	160K	32x48	1536	6144	316	2/24	Y	–	X	I/O	*
XCV400		10800	130K	282K-468K	230K	40x60	2400	9600	404	2/24	Y	–	X	I/O	*
XCV600		15552	187K	365K-661K	312K	48x72	3456	13824	512	2/24	Y	–	X	I/O	*
XCV800		21168	254K	511K-888K	406K	56x84	4704	18816	512	2/24	Y	–	X	I/O	*
XCV1000		27648	332K	622K-1,124K	512K	64x96	6144	24576	512	2/24	Y	–	X	I/O	*
XCV50E	Virtex-E Family: Density/ Performance Leadership BlockRAM Distributed RAM SelectI/O+ 8 DLLs LVDS, BLVDS, LVPECL	1728	21K	47K-72K	88K	16x24	384	2112	176	2/24	Y	X	I/O	I/O	*
XCV100E		2700	32K	105K-128K	117K	20x30	600	3120	176	2/24	Y	X	I/O	I/O	*
XCV200E		5292	64K	215K-306K	185K	28x42	1176	5712	284	2/24	Y	X	I/O	I/O	*
XCV300E		6912	83K	254K-412K	224K	32x48	1536	7296	316	2/24	Y	X	I/O	I/O	*
XCV400E		10800	130K	413K-570K	310K	40x60	2400	11040	404	2/24	Y	X	I/O	I/O	*
XCV600E		15552	187K	679K-986K	504K	48x72	3456	15552	512	2/24	Y	X	I/O	I/O	*
XCV1000E		27648	332K	1,146K-1,569K	768K	64x96	6144	26880	660	2/24	Y	X	I/O	I/O	*
XCV1600E		34992	420K	1,628K-2,189K	1062K	72x108	7776	33696	724	2/24	Y	X	I/O	I/O	*
XCV2000E		43200	518K	1,857K-2,542K	1240K	80x120	9600	41280	804	2/24	Y	X	I/O	I/O	*
XCV2600E		57132	686K	2,221K-3,264K	1529K	92x138	12696	54096	804	2/24	Y	X	I/O	I/O	*
XCV3200E		73008	876K	2,608K-4,047K	1846K	104x156	16224	68640	804	2/24	Y	X	I/O	I/O	*

* I/Os are 5 Volt compatible
X = Core and I/O voltage
I/Os = I/O voltage supported

Figure 2: FPGA Product Selection Matrix

High Density PROMs

Device	Density	PD8	SO20	PC20	VQ44	PC44	3 Volt	5 Volt	JTAG ISP
XC1701L	1Mb	X	X	X			X		
XC1701	1Mb	X	X	X				X	
XC1702L	2Mb				X		X		
XC1704L	4Mb				X		X		
XC17512L	512Kb	X	X	X			X		
XC18512	512Kb		X	X			X		X
XC1801	1Mb		X	X			X		X
XC1802	2Mb				X	X	X		X
XC1804	4Mb				X	X	X		X

3.3V Configuration PROMs for Spartan/Spartan-XL/Spartan-II

Device	Configuration Bits	PROM Solution	PD8	VO8	SO20	3 Volt	5 Volt
XCS05XL	54,544	XC17S05XL	X	X		X	
XCS10XL	95,752	XC17S10XL	X	X		X	
XC2S15	197,696	XC17S15XL	X	X		X	
XCS20XL	179,160	XC17S20XL	X	X		X	
XCS30XL	249,168	XC17S30XL	X	X		X	
XC2S30	336,768	XC17S30XL	X	X		X	
XCS40XL	330,696	XC17S40XL	X	X	X	X	
XC2S50	559,232	XC17S50XL	X		X	X	
XC2S100	781,248	XC17S100XL	X		X	X	
XC2S150	1,041,128	XC17S150XL	X		X	X	
XCS05	54,544	XC17S05	X	X			X
XCS10	95,752	XC17S10	X	X			X
XCS20	179,160	XC17S20	X	X			X
XCS30	249,168	XC17S30	X	X			X
XCS40	330,696	XC17S40	X		X		X

Configuration PROMs for Virtex

Device	Configuration Bits	XC17xx/18xx Solution	PD8	PC20	SO20	PC44	VQ44
XCV50	559,232	01	X*	X	X		
XCV100	781,248	01	X*	X	X		
XCV150	1,041,128	01	X*	X	X		
XCV200	1,335,872	02				X	X
XCV300	1,751,840	02				X	X
XCV400	2,546,080	04				X	X
XCV600	3,608,000	04				X	X
XCV800	4,715,648	04 + 512 or 8**				X	X
XCV1000	6,127,776	04 + 02 or 8**				X	X

* Available on XC17xx only
** In development

Configuration PROMs for Virtex-E

Device	Configuration Bits	XC17xx/18xx Solution	PD8	PC20	SO20	PC44	VQ44
XCV50E	630,048	01	X*	X	X		
XCV100E	863,840	01	X*	X	X		
XCV200E	1,442,106	01	X*	X	X		
XCV300E	1,875,648	02				X	X
XCV400E	2,693,440	02				X	X
XCV600E	3,961,632	04				X	X
XCV1000E	6,587,520	04 + 02 or 8***				X	X
XCV1600E	8,308,992	04 + 04 or 8***				X	X
XCV2000E	10,159,648	08 + 04 or 16***				X	X
XCV2600E	12,923,000**	16***				X	X
XCV3200E	16,284,000**	16***				X	X

* Available on XC17xx only
** Estimated
*** In development

Low Density PROMs

Device	Density	PD8	SO8	VO8	SO20	PC20	3 Volt	5 Volt	JTAG ISP
XC1736E	36Kb	X	X	X		X		X	
XC1765E	64Kb	X	X	X		X		X	
XC1765EL(X)	64Kb	X	X	X		X	X		
XC17128E	128Kb	X		X		X		X	
XC17128EL(X)	128Kb	X		X		X	X		
XC17256E	256Kb	X		X		X		X	
XC17256EL(X)	256Kb	X		X		X	X		
XC18128	128Kb				X	X	X		X
XC18256	256Kb				X	X	X		X

Note: XC1700EL parts are marked with an "X" instead of "EL"

Figure 3: PROM Package Options and Product Selection

CPLD Package Options and User I/O																										
		XC9536	XC9572	XC95108	XC95144	XC95216	XC95288	XC9536XL	XC9572XL	XC95144XL	XC95288XL	XCR22LV10	XCR22V10	XCR3032A	XCR3064A	XCR3128A	XCR3320C	XCR3960C	XCR5032C	XCR5064C	XCR5128C	XCR3032XL*	XCR3064XL	XCR3128XL	XCR3256XL	XCR3384XL*
	I/O	34	72	108	133	166	192	36	72	117	192	10	10	32	64	96	192	384	32	64	96	32	64	104	160	216
PLCC																										
	28											10	10													
	44	34	34					34	34					32	32				32	32						
	84		69	69																						
VQFP																										
	44	34						34	34					32	32				32	32		32	32			
	64							36	52																	
	100														64	80				64	80		64	80		
CSP																										
	48	34						36	38													32				
	56														44								44			
	144									117														104		
	280										192														160	216
TQFP																										
	100		72	81	81				72	81																
	128															96					96					
	144									117	117													104	104	
	160																112									
PQFP																										
	100		72	81	81																					
	160			108	133	133																				
	208										168														160	
HQFP																										
	208					166	168																			
BGA																										
	256										192						192									
	352					166	192																			
	492																	384								
SOL																										
	24											10	10													
TSSOP																										
	24											10	10													
FBGA																										
	256										192															

* Contact sales offices for up-to-date product and package availability

Figure 4: CPLD Package Options and User I/O

				Density		Features				
Core Voltage	CPLD Family	Devices	Key Features	Macrocells	Max. I/O	Pin-to-Pin Delay (ns)	System Frequency	Individual OE Ctrl	JTAG	Ultra Low-Power
3.3 Volt ISP	XC9500XL	XC9536XL	Best Pin-Locking JTAG w/Clamp High Performance High Endurance	36	36	5	200	✓	✓	
		XC9572XL		72	72	5	178.6	✓	✓	
		XC95144XL		144	117	5	178.6	✓	✓	
		XC95288XL		288	192	7	151	✓	✓	
	XPLA3	XCR3032XL	Ultra Low Power JTAG Increased Logic Flexibility	32	32	5	200		✓	✓
		XCR3064XL		64	64	6	166		✓	✓
		XCR3128XL		128	104	6	166		✓	✓
		XCR3256XL		256	160	7.5	133		✓	✓
		XCR3384XL		384	216	7.5	133		✓	✓
	XPLA-Enhanced	XCR3032A (PZ3032A)*	Ultra Low Power JTAG	32	32	6	111		✓	✓
		XCR3064A (PZ3064A)*		64	64	7.5	95		✓	✓
		XCR3128A (PZ3128A)*		128	96	7.5	95		✓	✓
	XPLA2	XCR3320 (PZ3320C)*	Ultra Low Power High Density	320	192	7.5	100		✓	✓
		XCR3960 (PZ3960C)*		960	384	7.5	100		✓	✓
5 Volt ISP	XC9500	XC9536	Best Pin-Locking JTAG High Endurance	36	34	5	100	✓	✓	
		XC9572		72	72	7.5	83.3	✓	✓	
		XC95108		108	108	7.5	83.3	✓	✓	
		XC95144		144	133	7.5	83.3	✓	✓	
		XC95216		216	166	10	66.7	✓	✓	
		XC95288		288	192	10	66.7	✓	✓	
	XPLA-Enhanced	XCR5032C (PZ5032C)*	Ultra Low Power JTAG	32	32	6	111		✓	✓
		XCR5064C (PZ5064C)*		64	64	7.5	105		✓	✓
		XCR5128C (PZ5128C)*		128	96	7.5	100		✓	✓

* Philips part number

Figure 5: CPLD Product Selection Matrix