Development Systems: Products Overview

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Introduction

Leading-edge silicon products, state-of-the art software solutions and world-class technical support make up the total solution delivered by Xilinx. The software component of this solution is critical to the success of every design project. Xilinx Software Solutions provide powerful tools which make designing with programmable logic simple. Push button design flows, integrated on-line help, multimedia tutorials, plus high performance automatic and auto-interactive tools, help designers achieve optimum results. And the industry's broadest array of programmable logic technology and EDA integration options deliver unparalleled design flexibility.

Product Overview

Xilinx Software Solutions are available in two different product series making it easy for designers to choose the right system for their needs. These two series support the industry's broadest array of programmable logic IC families. This allows users to standardize their design tools for all programmable logic applications and use these tools to realize the benefits of the industry's highest performance and density FPGAs and CPLDs. It also makes it easy to migrate designs to new technologies and re-use existing designs in new applications.

The **Xilinx Foundation Series** provides designers with a complete, ready-to-use solution for programmable logic design.

The **Xilinx Alliance Series** provides designers powerful integration of Xilinx design tools with their existing EDA environment.

Flexible Configurations

Xilinx Software Solutions are available in three device configurations giving designers a cost-effective way to match their tools to the design methodologies they require. These configurations are available for both the Foundation and Alliance Series.

Base configurations provide push button design flows and support a broad array of FPGA and CPLD devices targeted for low density and high volume applications.

Standard configurations combine push button flows with powerful auto-interactive tools. These tools give designers more influence and control over implementation while maintaining the benefits of design automation. Standard configurations include support for all Xilinx programmable logic devices up to and including one million gates.

Elite configurations created to deliver the powerful design tools necessary for designers when creating designs for our greater than one million gate devices.

Foundation Series

The Xilinx Foundation Series provides everything required to design a programmable logic device in an easy-to-use environment. This fully integrated tool set allows users to access design entry, synthesis, implementation and simulation tools in a ready-to-use package. Every step in the design process is accomplished using graphical tool bars, icons and pop-up menus supported by interactive tutorials and comprehensive on-line help.

The Xilinx Foundation Series features support for standards based HDL design. All configurations support the popular ABEL language, with integrated compilers optimized for each target architecture. HDL configurations include integrated VHDL/Verilog synthesis from Synopsys with tutorials and graphical HDL design entry tools to turn new users into experts quickly and easily.

Configurations

Configurations of the Foundation Series contain integrated VHDL/Verilog synthesis and graphical interactive HDL entry tools with the following features:

On-line tutorial teaches the art of VHDL design.

Xilinx HDL Editor provides color coding, syntax checking and single click error navigation making it easy to create and debug VHDL, Verilog and ABEL designs.

Graphical State Machine editor makes the design of simple or complex state machines simple and intuitive.

HDL Language Assistant provides libraries of common functions with optimized VHDL, Verilog and ABEL code.

FPGA and CPLD specific synthesis and optimization from Synopsys tools produce high-utilization, high-performance results.

Foundation iSE v3.1I

http://www.xilinx.com/products/found.htm

The Foundation iSE software has been designed to enable both new and experienced Programmable logic designers to achieve results, through intuitive design flows. You are assured of success on each and every design because Foundation Series gives you the advanced tools and technology you need.

The Foundation iSE software represents Xilinx next evolution of our software. Xilinx has created a powerful HDL design environment by integrating and further developing acquired technology with our own FPGA design tools and powerful implementation tools. You will benefit from the same powerful tools and features of our Foundation and Alliance tools while working in a new environment designed to help you work faster and more efficiently.

The iSE software is packaged with two powerful synthesis tools: the FPGA Express from Synopsys and our own XST (Xilinx Synthesis Technology). We understand that synthesis tools work differently on different designs, with multiple synthesis tools you will have the option of using the tool that fits your design needs. The Foundation iSE Software comes in three configurations:

- Base X
- Express
- Elite

Alliance Series

The Alliance Series provides powerful and integrated design tools for users who require a quality solution for their chosen EDA design solution. With the Alliance Series, users can choose from a wide range of design techniques including schematic capture, module-based design and HDL design solutions. With standard based design interfaces including EDIF, VITAL, VHDL, Verilog and SDF, this series provides maximum flexibility, portability, mixed vendor support, and design reuse.

Quality integration with leading EDA vendors such as ALDEC, Exemplar, Cadence, Mentor Graphics, Model Technology, OrCAD, Synopsys, Synplicity, Veribest and VIEWlogic provide tightly-coupled environments that make it easy to move through the design process and through a mixed EDA vendor flow. The EDA vendors are supported through the Xilinx Alliance Program, insuring high quality tools and accuracy of results. Information on Xilinx Alliance Program vendors can be found on the Xilinx WEB page **www.xilinx.com.**

The Alliance design solutions continue Xilinx' trend of cutting place and route runtime in half, while maintaining or improving design performance. The accumulation of runtime improvements now enable the compilation of the 100,000 system gate Virtex devices in less time. Fast compile times translate to more turns per day and greater productivity.

Features include:

Timing Driven Place and Route. Allows you to specify your timing requirements for critical paths. This feature often gives 30-40% performance improvements when speed is critical; you no longer need to manually fine-tune your design.

Static Timing Analysis. Shortens your design process by providing an evaluation of your timing at various points in the implementation process, allowing you to make changes immediately.

Flow Engine. Automates and simplifies the implementation process. Using a simple graphical interface, you can monitor and control all aspects of your design implementation.

Simulation. Provides design verification before and after implementation, thus reducing the number of design iterations required to meet design specifications.

Incremental Design Capability. Reduces your overall design cycle by allowing you to re-use previous iterations of your design. This is very helpful for evaluating design alterations.

Hierarchical Timing Analysis. The Interactive Timing Analyzer has received a variety of dramatic improvements to its User interface, including hierarchical reporting of timing analysis results. This feature simplifies the process of navigation through the rich set of timing information Xilinx provides on your design. The Alliance Software comes in two configurations:

- Standard
- Elite

ModelSim Xilinx Edition

(http://www.xilinx.com/products/software/mxe.htm)

The ModelSim Xilinx Edition (XE) simulator is a complete HDL simulation environment, optimized for use in verifying Xilinx programmable logic designs. ModelSim XE enables designers to verify source code (VHDL and Verilog), functional, and timing models of their design using a common "self-checking" testbench. ModelSim XE provides a powerful first step into the world of HDL simulation with capacity and performance designed for the verification of the Xilinx XC9500 CPLD and Spartan FPGA series of programmable logic devices as well as lower-density XC4000 and Virtex series FPGAs.

ModelSim XE is most valuable for customers who understand the benefits of VHDL or Verilog simulation, and are looking for a cost-effective solution for low-density programmable logic design. It is available in both VHDL and Verilog versions. ModelSim XE may only be used with v2.1i Xilinx development systems and later. Xilinx sells the MOD-

ELSIM XE products as options to any of its development systems.

CPLD Web Powered Software Solutions:

The Xilinx CPLD Web Powered Software Solutions offer designers the flexibility to do CPLD design evaluation and fitting on-line or on their desktop. The WebFITTER is an on-line device fitting and evaluation tool which accepts VHDL, Verilog, ABEL or netlist files. The WebPACK downloadable desktop solutions offer FREE CPLD software modules from ABEL and HDL synthesis to device fitting and JTAG programming.

WebFITTER:

(http://www.xilinx.com/sxpresso/webfitter.htm)

The Xilinx WebFITTER is a FREE, web-based CPLD design evaluation and fitting software tool that allows system designers to target their designs using the industry's best CPLDs, the XC9500 Series and the CoolRunner Series, on the latest version of Xilinx software and get their results and pricing in minutes!

WebPACK:

(http://www.xilinx.com/sxpresso/webpack.htm)

The Xilinx WebPACK contains FREE downloadable software solutions for Xilinx XC9500 and CoolRunner Series CPLDs. Each solution provides a simple andintuitive design environment for any Xilinx CPLD family. The WebPACK is a collection of three design suites: design entry, device fitting and programming. These tools can be downloaded and used individually or, when installed together become an integrated design environment for Xilinx CPLDs.