XCR5032: 32 Macrocell CPLD

DS045 (v1.1) February 10, 2000 Product Specification

Features

- Industry's first TotalCMOS™ PLD - both CMOS design and process technologies
- Fast Zero Power (FZP™) design technique provides ultra-low power and very high speed
- High speed pin-to-pin delays of 6 ns
- Ultra-low static power of less than 75 µA
- 100% routable with 100% utilization while all pins and all macrocells are fixed
- Deterministic timing model that is extremely simple to use
- Two clocks with programmable polarity at every macrocell
- Support for asynchronous clocking
- Innovative XPLA™ architecture combines high speed with extreme flexibility
- 1000 erase/program cycles guaranteed
- 20 years data retention guaranteed
- Logic expandable to 37 product terms
- PCI compliant
- Advanced 0.5µ E^2CMOS process
- Security bit prevents unauthorized access
- Design entry and verification using industry standard and Xilinx CAE tools
- Reprogrammable using industry standard device programmers
- Innovative Control Term structure provides either sum terms or product terms in each logic block for:
  - Programmable 3-state buffer
  - Asynchronous macrocell register preset/reset
- Programmable global 3-state pin facilitates `bed of nails' testing without using logic resources
- Available in both PLCC and VQFP packages
- Available in both Commercial and Industrial grades

Description

The XCR5032 CPLD (Complex Programmable Logic Device) is the first in a family of CoolRunner™ CPLDs from Xilinx. These devices combine high speed and zero power in a 32 macrocell CPLD. With the FZP design technique, the XCR5032 offers true pin-to-pin speeds of 6 ns, while simultaneously delivering power that is less than 75 µA at standby without the need for "turbo bits" or other power down schemes. By replacing conventional sense amplifier methods for implementing product terms (a technique that has been used in PLDs since the bipolar era) with a cascaded chain of pure CMOS gates, the dynamic power is also substantially lower than any competing CPLD. These devices are the first TotalCMOS PLDs, as they use both a CMOS process technology **and** the patented full CMOS FZP design technique. For 3V applications, Xilinx also offers the high speed XCR3032 CPLD that offers these features in a full 3V implementation.

The Xilinx FZP CPLDs utilize the patented XPLA (eXtended Programmable Logic Array) architecture. The XPLA architecture combines the best features of both PLA and PAL type structures to deliver high speed and flexible logic allocation that results in superior ability to make design changes with fixed pinouts. The XPLA structure in each logic block provides a fast 6 ns PAL path with five dedicated product terms per output. This PAL path is joined by an additional PLA structure that deploys a pool of 32 product terms to a fully programmable OR array that can allocate the PLA product terms to any output in the logic block. This combination allows logic to be allocated efficiently throughout the logic block and supports as many as 37 product terms on an output. The speed with which logic is allocated from the PLA array to an output is only 2 ns, regardless of the number of PLA product terms used, which results in worst case t_{PD}'s of only 8 ns from any pin to any other pin. In addition, logic that is common to multiple outputs can be placed on a single PLA product term and shared across multiple outputs via the OR array, effectively increasing design density.

The XCR5032 CPLDs are supported by industry standard CAE tools (Cadence/OrCAD, Exemplar Logic, Mentor, Synopsys, Synario, Viewlogic, and Synplicity), using text (ABEL, VHDL, Verilog) and/or schematic entry. Design verification uses industry standard simulators for functional and timing simulation. Development is supported on personal computer, Sparc, and HP platforms. Device fitting uses a Xilinx developed tool, XPLA Professional (available on the Xilinx web site).

The XCR5032 CPLD is reprogrammable using industry standard device programmers from vendors such as Data I/O, BP Microsystems, SMS, and others.

XPLA Architecture

Figure 1shows a high level block diagram of a 32 macrocell device implementing the XPLA architecture. The XPLA architecture consists of logic blocks that are interconnected by a Zero-power Interconnect Array (ZIA). The ZIA is a virtual crosspoint switch. Each logic block is essentially a 36V16 device with 36 inputs from the ZIA and 16 macrocells. Each logic block also provides 32 ZIA feedback paths from the macrocells and I/O pins.

From this point of view, this architecture looks like many other CPLD architectures. What makes the CoolRunner family unique is what is inside each logic block and the design technique used to implement these logic blocks. The contents of the logic block will be described next.

Logic Block Architecture

Figure 2 illustrates the logic block architecture. Each logic block contains control terms, a PAL array, a PLA array, and 16 macrocells. the six control terms can individually be configured as either SUM or PRODUCT terms, and are used to control the preset/reset and output enables of the 16 macrocells' flip-flops. The PAL array consists of a programmable AND array with a fixed OR array, while the PLA array consists of a programmable AND array with a programmable OR array. The PAL array provides a high speed path through the array, while the PLA array provides increased product term density.

Each macrocell has five dedicated product terms from the PAL array. The pin-to-pin t_{PD} of the XCR5032 device through the PAL array is 6 ns. This performance is equivalent to the fastest 5V CPLD available today. If a macrocell needs more than five product terms, it simply gets the additional product terms from the PLA array. The PLA array consists of 32 product terms, which are available for use by all 16 macrocells. The additional propagation delay incurred by a macrocell using one or all 32 PLA product terms is just 2 ns. So the total pin-to-pin t_{PD} for the XCR5032 using six to 37 product terms is 8 ns (6 ns for the PAL + 2 ns for the PLA).

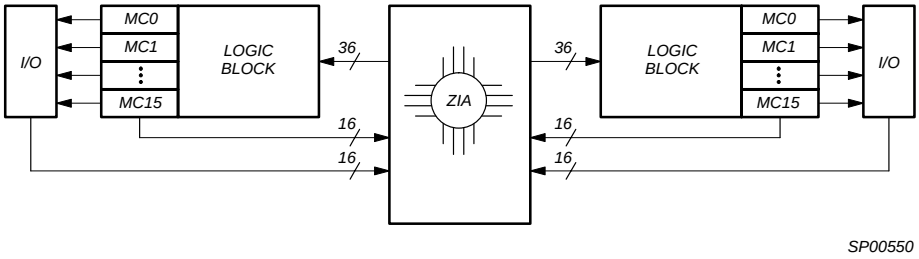


Figure 1: Xilinx XPLA CPLD Architecture

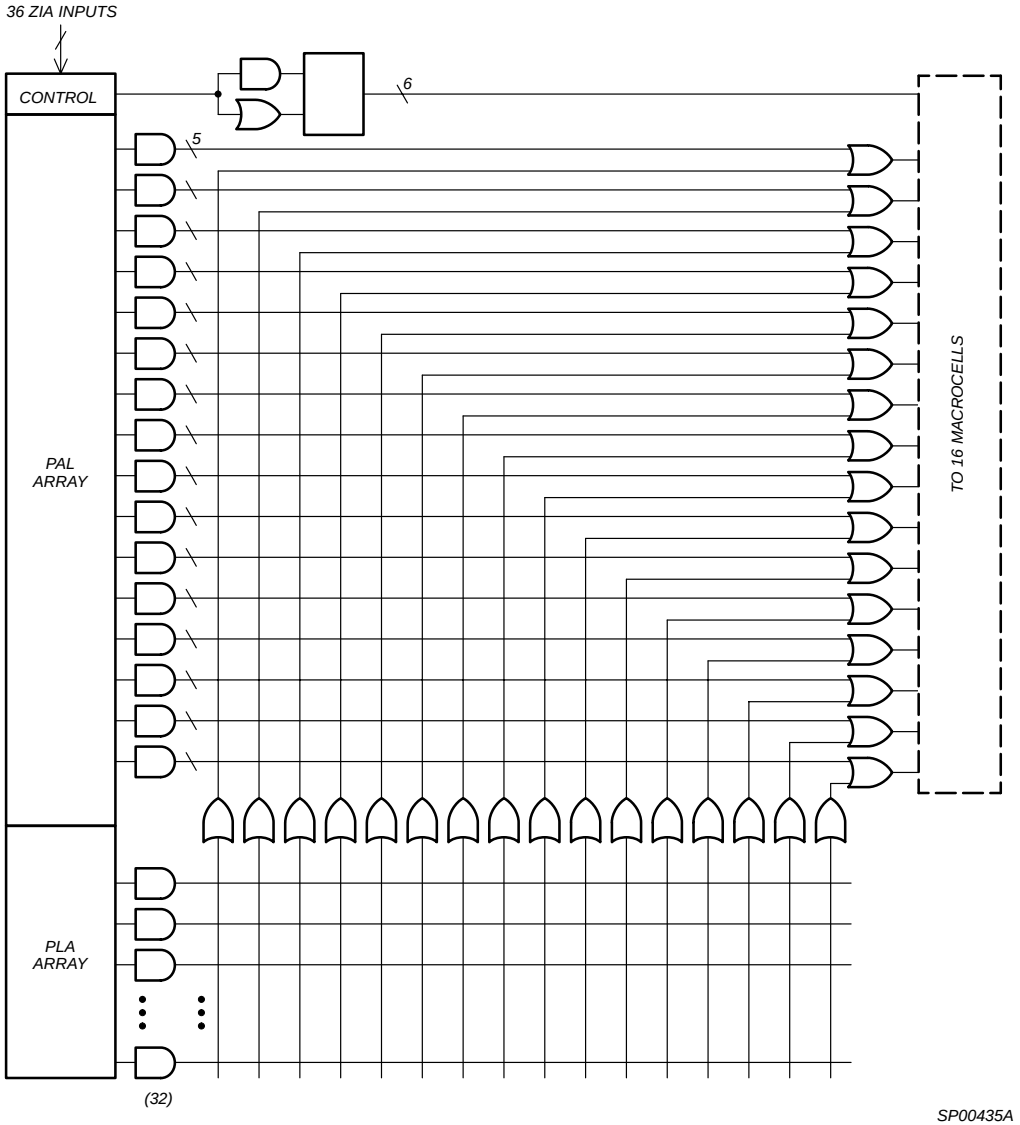


Figure 2: Xilinx XPLA Logic Block Architecture

Macrocell Architecture

Figure 2 shows the architecture of the macrocell used in the CoolRunner family. The macrocell consists of a flip-flop that can be configured as either a D- or T-type. A D-type flip-flop is generally more useful for implementing state machines and data buffering. A T-type flip-flop is generally more useful in implementing counters. All CoolRunner family members provide both synchronous and asynchronous clocking and provide the ability to clock off either the falling or rising edges of these clocks. These devices are designed such that the skew between the rising and falling edges of a clock are minimized for clocking integrity. There are two clocks (CLK0 and CLK1) available on the XCR5032 device. Clock 0 (CLK0) is designated as the "synchronous" clock and must be driven by an external source. Clock 1 (CLK1) can either be used as a synchronous clock (driven by an external source) or as an asynchronous clock (driven by a macrocell equation). The timing for asynchronous clocks is different in that the t_{CO} time is extended by the amount of time that it takes for the signal to propagate through the array and reach the clock network, and the t_{SU} time is reduced.

Two of the control terms (CT0 and CT1) are used to control the Preset/Reset of the macrocell's flip-flop. The Preset/Reset feature for each macrocell can also be disabled. Note that the Power-on Reset leaves all macrocells in the "zero" state when power is properly applied. The other four-control terms (CT2-CT5) can be used to control the Output Enable of the macrocell's output buffers. The reason there are as many control terms dedicated for the Output Enable of the macrocell is to insure that all CoolRunner devices are PCI compliant. The macrocell's output buffers can also be always enabled or disabled. All CoolRunner devices also provide a Global 3-State (GTS) pin, which, when enabled and pulled Low, will 3-state all the outputs of the device. This pin is provided to support "In-Circuit Testing" or "Bed-of-Nails" testing.

There are two feedback paths to the ZIA: one from the macrocell, and one from the I/O pin. The ZIA feedback path before the output buffer is the macrocell feedback path, while the ZIA feedback path after the output buffer is the I/O pin ZIA path. When the macrocell is used as an output, the output buffer is enabled, and the macrocell feedback path can be used to feedback the logic implemented in the macrocell. When the I/O pin is used as an input, the output buffer will be 3-stated and the input signal will be fed into the ZIA via the I/O feedback path, and the logic implemented in the buried macrocell can be fed back to the ZIA via the macrocell feedback path. It should be noted that unused inputs or I/Os should be properly terminated.

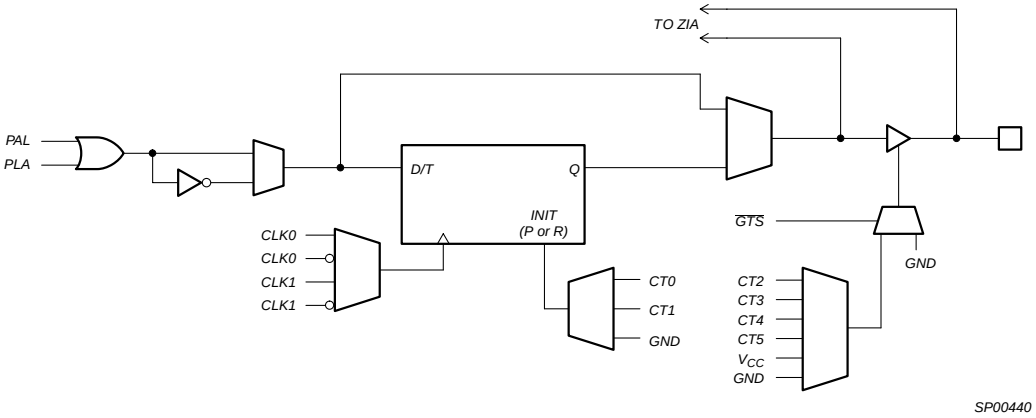


Figure 2: XCR5032 Macrocell Architecture

Terminations

The CoolRunner XCR5032C CPLDs are TotalCMOS devices. As with other CMOS devices, it is important to consider how to properly terminate unused inputs and I/O pins when fabricating a PC board. The XCR5032C devices do not have on-chip termination circuits, so it is recommended that unused inputs and I/O pins be properly terminated. Allowing unused inputs and I/O pins to float can cause the voltage to be in the linear region of the CMOS input structures, which can increase the power consumption of the device. Xilinx recommends the use of 10KΩ pull-up resistors for the termination. Using pull-up resistors allows the flexibility of using these pins should late design changes require additional I/O. These unused pins may also be tied directly to V_{CC}, but this will make it more difficult to reclaim the use of the pin, should this be needed by a subsequent design revision.See the application note *Terminating Unused I/O Pins in Xilinx XPLA1 and XPLA2 CoolRunner CPLDs* for more information.

Simple Timing Model

Figure 3 shows the CoolRunner Timing Model. The CoolRunner timing model looks very much like a 22V10 timing model in that there are three main timing parameters, including t_{PD}, t_{SU}, and t_{CO}. In other architectures, the user may be able to fit the design into the CPLD, but is not sure whether system timing requirements can be met until after the design has been fit into the device. This is because the timing models of competing architectures are very complex and include such things as timing dependencies on the number of parallel expanders borrowed, sharable expanders, varying number of X and Y routing channels used, etc. In the XPLA architecture, the user knows up front whether the design will meet system timing requirements. This is due to the simplicity of the timing model. For example, in the XCR5032 device, the user knows up front that if a given output uses five product terms or less, the t_{PD} = 6 ns, the t_{SU} = 4.5 ns, and the t_{CO} = 5 ns. If an output is using six to 37 product terms, an additional 2 ns must be added to the t_{PD} and t_{SU} timing parameters to account for the time to propagate through the PLA array.

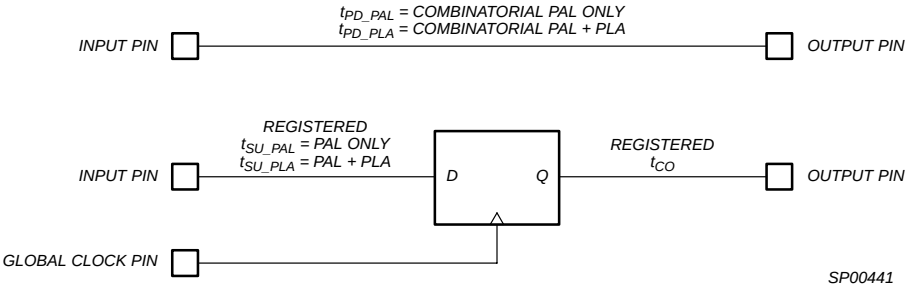
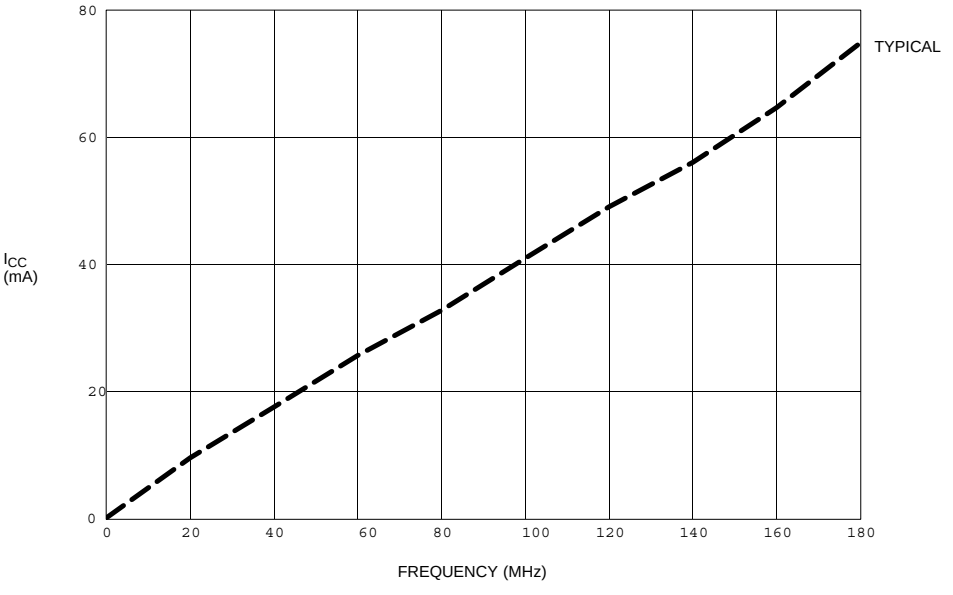


Figure 3: CoolRunner Timing Model

TotalCMOS Design Technique for Fast Zero Power

Xilinx is the first to offer a TotalCMOS CPLD, both in process technology and design technique. Xilinx employs a cascade of CMOS gates to implement its Sum of Products instead of the traditional sense amp approach. This CMOS gate implementation allows Xilinx to offer CPLDs which are both high performance and low power, breaking the paradigm that to have low power, you must have low performance. Refer to Figure 4 and Table 1 showing the I_{CC} vs. Frequency of our XCR5032 TotalCMOS CPLD.



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I_{CC} vs. Frequency at 5V, 25°C

Table 1: I_{CC} vs Frequency (V_{CC} = 5V, 25°C)

Frequency (MHz)	0	20	40	60	80	100	120	140	160	180
Typical I_{CC} (mA)	0.05	9.62	17.5	25.6	32.5	40.8	49.0	55.9	64.2	75.2

Absolute Maximum Ratings[1]

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage[2]	-0.5	7.0	V
V_I	Input voltage	-1.2	V_{CC} +0.5	V
V_{OUT}	Output voltage	-0.5	V_{CC} +0.5	V
I_{IN}	Input current	-30	30	mA
I_{OUT}	Output current	-100	100	mA
T_J	Maximum junction temperature	-40	150	°C
T_{str}	Storage temperature	-65	150	°C

Notes:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification is not implied.
2. The chip supply voltage must rise monotonically.

Operating Range

Product Grade	Temperature	Voltage
Commercial	0 to +70°C	5V +5%
Industrial	-40 to +85°C	5V +10%

DC Electrical Characteristics For Commercial Grade Devices

Commercial: $0°C \le T_{AMB} \le +70°C$; $4.75V \le V_{CC} \le 5.25V$

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{IL}	Input voltage low	V_{CC} = 4.75V		0.8	V
V_{IH}	Input voltage high	V_{CC} = 5.25V	2.0		V
V_I	Input clamp voltage	V_{CC} = 4.75V, I_{IN} = -18 mA		-1.2	V
V_{OL}	Output voltage low	V_{CC} = 4.75V, I_{OL} = 12 mA		0.5	V
V_{OH}	Output voltage high	V_{CC} = 4.75V, I_{OH} = -12 mA	2.4		V
I_{IL}	Input leakage current low	V_{CC} = 5.25V (except CKO), V_{IN} = 0.4V	-10	10	µA
I_{IH}	Input leakage current high	V_{CC} = 5.25V, V_{IN} = 3.0V	-10	10	µA
I_{IL}	Clock input leakage current	V_{CC} = 5.25V, V_{IN} = 0.4V	-10	10	µA
I_{OZL}	3-stated output leakage current low	V_{CC} = 5.25V, V_{IN} = 0.4V	-10	10	µA
I_{OZH}	3-stated output leakage current high	V_{CC} = 5.25V, V_{IN} = 3.0V	-10	10	µA
I_{CCQ}[1]	Standby current	V_{CC} = 5.25V, T_{AMB} = 0°C		75	µA
I_{CCD}[1, 2]	Dynamic current	V_{CC} = 5.25V, T_{AMB} = 0°C at 1 MHz		3	mA
		V_{CC} = 5.25V, T_{AMB} = 0°C at 50 MHz		30	mA
I_{OS}	Short circuit output current[3]	One pin at a time for no longer than 1 second	-50	-200	mA
C_{IN}	Input pin capacitance[3]	T_{AMB} = 25°C, f = 1 MHz		8	pF
C_{CLK}	Clock input capacitance[3]	T_{AMB} = 25°C, f = 1 MHz	5	12	pF
$C_{I/O}$	I/O pin capacitance[3]	T_{AMB} = 25°C, f = 1 MHz		10	pF

Notes:

1. See Table 1 on page 6 for typical values.
2. This parameter measured with a 16-bit, loadable up/down counter loaded into every logic block, with all outputs enabled and unloaded. Inputs are tied to V_{CC} or ground. This parameter guaranteed by design and characterization, not testing.
3. Typical values, not tested.

AC Electrical Characteristics[1] For Commercial Grade Devices

Commercial: 0°C ≤ T_{AMB} ≤ +70°C; 4.75V ≤ V_{CC} ≤ 5.25V

Symbol	Parameter	6		7		10		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD_PAL}	Propagation delay time, input (or feedback node) to output through PAL	2	6	2	7.5	2	10	ns
t_{PD_PLA}	Propagation delay time, input (or feedback node) to output through PAL + PLA	3	8	3	10	3	12.5	ns
t_{CO}	Clock to out (global synchronous clock from pin)	2	5.5	2	7	2	9	ns
t_{SU_PAL}	Setup time (from input or feedback node) through PAL	4		5.5		8		ns
t_{SU_PLA}	Setup time (from input or feedback node) through PAL + PLA	6		8		10.5		ns
t_H	Hold time		0		0		0	ns
t_{CH}	Clock High time	3		4		5		ns
t_{CL}	Clock Low time	3		4		5		ns
t_R	Input rise time		20		20		20	ns
t_F	Input fall time		20		20		20	ns
f_{MAX1}	Maximum FF toggle rate[2] ($1/t_{CH} + t_{CL}$)	167		125		100		MHz
f_{MAX2}	Maximum internal frequency[2] ($1/t_{SUPAL} + t_{CF}$)	125		91		64		MHz
f_{MAX3}	Maximum external frequency[2] ($1/t_{SUPAL} + t_{CO}$)	105		80		59		MHz
t_{BUF}	Output buffer delay time		1.5		1.5		1.5	ns
t_{PDF_PAL}	Input (or feedback node) to internal feedback node delay time through PAL		4.5		6		8.5	ns
t_{PDF_PLA}	Input (or feedback node) to internal feedback node delay time through PAL + PLA		6.5		8.5		11	ns
t_{CF}	Clock to internal feedback node delay time		4		5.5		7.5	ns
t_{INIT}	Delay from valid V_{CC} to valid reset		50		50		50	µs
t_{ER}	Input to output disable[2, 3]		11		12.5		15	ns
t_{EA}	Input to output valid[2]		11		12.5		15	ns
t_{RP}	Input to register preset[2]		11		12.5		15	ns
t_{RR}	Input to register reset[2]		14		15.5		18	ns

Notes:

1. Specifications measured with one output switching. See Figure 5 and Table 2 for derating.
2. This parameter guaranteed by design and characterization, not by test.
3. Output C_L = 5 pF.

DC Electrical Characteristics For Industrial Grade Devices

Industrial: -40°C ≤ T_{AMB} ≤ +85°C; 4.5V ≤ V_{CC} ≤ 5.5V

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{IL}	Input voltage low	V_{CC} = 4.5V		0.8	V
V_{IH}	Input voltage high	V_{CC} = 5.5V	2.0		V
V_I	Input clamp voltage	V_{CC} = 4.5V, I_{IN} = -18 mA		-1.2	V
V_{OL}	Output voltage low	V_{CC} = 4.5V, I_{OL} = 12 mA		0.5	V
V_{OH}	Output voltage high	V_{CC} = 4.5V, I_{OH} = -12 mA	2.4		V
I_{IL}	Input leakage current low	V_{CC} = 5.5V (except CKO), V_{IN} = 0.4V	-10	10	µA
I_{IH}	Input leakage current high	V_{CC}= 5.5V, V_{IN} = 3.0V	-10	10	µA
I_{IL}	Clock input leakage current	V_{CC} = 5.5V, V_{IN} = 0.4V	-10	10	µA
I_{OZL}	3-stated output leakage current low	V_{CC}= 5.5V, V_{IN} = 0.4V	-10	10	µA
I_{OZH}	3-stated output leakage current high	V_{CC} = 5.5V, V_{IN} = 3.0V	-10	10	µA
I_{CCQ}[1]	Standby current	V_{CC} = 5.5V, T_{AMB} = -40°C		95	µA
I_{CCD}[1, 2]	Dynamic current	V_{CC} = 5.5V, T_{AMB} = -40°C at 1 MHz		4	mA
		V_{CC} = 5.5V, T_{AMB} = -40°C at 50 MHz		35	mA
I_{OS}	Short circuit output current[3]	One pin at a time for no longer than 1 second	-50	-230	mA
C_{IN}	Input pin capacitance[3]	T_{AMB} = 25°C, f = 1 MHz		8	pF
C_{CLK}	Clock input capacitance[3]	T_{AMB} = 25°C, f = 1 MHz	5	12	pF
$C_{I/O}$	I/O pin capacitance[3]	T_{AMB} = 25°C, f = 1 MHz		10	pF

Notes:

1. See Table 1 on page 6 for typical values.
2. This parameter measured with a 16-bit, loadable up/down counter loaded into every logic block, with all outputs enabled and unloaded. Inputs are tied to V_{CC} or ground. This parameter guaranteed by design and characterization, not testing.
3. Typical values, not tested.

AC Electrical Characteristics[1] For Industrial Grade Devices

Industrial: -40°C ≤ T_{AMB} ≤ +85°C; 4.5V ≤ V_{CC} ≤ 5.5V

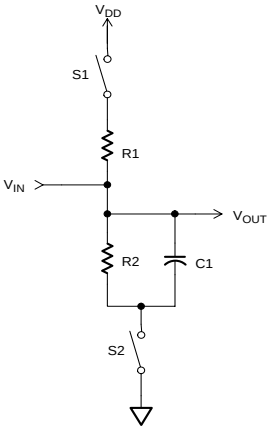
Symbol	Parameter	7		10		Unit
		Min.	Max.	Min.	Max.	
t_{PD_PAL}	Propagation delay time, input (or feedback node) to output through PAL	2	7.5	2	10	ns
t_{PD_PLA}	Propagation delay time, input (or feedback node) to output through PAL + PLA	3	9.5	3	12.5	ns
t_{CO}	Clock to out (global synchronous clock from pin)	2	6	2	9	ns
t_{SU_PAL}	Setup time (from input or feedback node) through PAL	5		8		ns
t_{SU_PLA}	Setup time (from input or feedback node) through PAL + PLA	7		10.5		ns
t_H	Hold time		0		0	ns
t_{CH}	Clock High time	4		5		ns
t_{CL}	Clock Low time	4		5		ns
t_R	Input rise time		20		20	ns
t_F	Input fall time		20		20	ns
f_{MAX1}	Maximum FF toggle rate[2] ($1/t_{CH} + t_{CL}$)	125		100		MHz
f_{MAX2}	Maximum internal frequency[2] ($1/t_{SUPAL} + t_{CF}$)	105		64		MHz
f_{MAX3}	Maximum external frequency[2] ($1/t_{SUPAL} + t_{CO}$)	91		59		MHz
t_{BUF}	Output buffer delay time		1.5		1.5	ns
t_{PDF_PAL}	Input (or feedback node) to internal feedback node delay time through PAL		6		8.5	ns
t_{PDF_PLA}	Input (or feedback node) to internal feedback node delay time through PAL+PLA		8		11	ns
t_{CF}	Clock to internal feedback node delay time		4.5		7.5	ns
t_{INIT}	Delay from valid V_{CC} to valid reset		50		50	µs
t_{ER}	Input to output disable[2, 3]		12		15	ns
t_{EA}	Input to output valid[2]		12		15	ns
t_{RP}	Input to register preset[2]		12		15	ns
t_{RR}	Input to register reset[2]		14		18	ns

Notes:

1. Specifications measured with one output switching. See Figure 5 and Table 2 for derating.
2. This parameter guaranteed by design and characterization, not by test.
3. Output C_L = 5 pF.

Switching Characteristics

The test load circuit and load values for the AC Electrical Characteristics are illustrated below.



COMPONENT	VALUES
R1	470Ω
R2	250Ω
C1	35 pF

MEASUREMENT	S1	S2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Closed
t_P	Closed	Closed

NOTE: For t_{PHZ} and t_{PLZ} C = 5pF, and 3-State levels are measured 0.5V from steady state active level.

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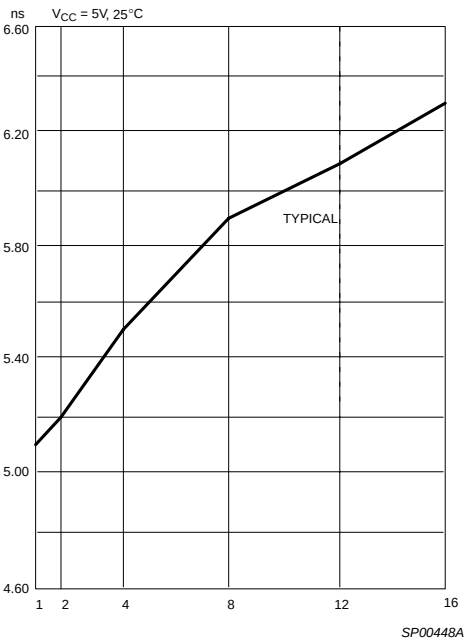

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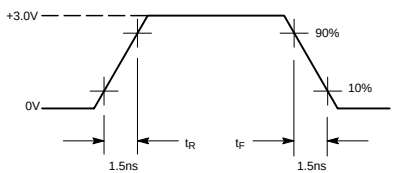
Figure 5: t_{PD_PAL} vs Outputs Switching

Voltage Waveform



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MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

Table 2: t_{PD_PAL} vs # of Outputs switching (V_{CC} = 5V)

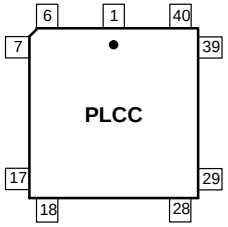
# of Outputs	1	2	4	8	12	16
Typical (ns)	5.1	5.2	5.5	5.9	6.1	6.3

Pin Function and Layout

Pin Functions

Pin #	PLCC	VQFP	Pin #	PLCC	VQFP
1	IN1	I/O-A3	23	V_{CC}	I/O-B10
2	IN3	I/O-A4	24	I/O-B15	GND
3	V_{CC}	I/O-A5	25	I/O-B14	I/O-B9
4	I/O-A0-CK1	GND	26	I/O-B13	I/O-B8
5	I/O-A1	I/O-A6	27	I/O-B12	I/O-B7
6	I/O-A2	I/O-A7	28	I/O-B11	I/O-B6
7	I/O-A3	I/O-A8	29	I/O-B10	V_{CC}
8	I/O-A4	I/O-A9	30	GND	I/O-B5
9	I/O-A5	V_{CC}	31	I/O-B9	I/O-B4
10	GND	I/O-A10	32	I/O-B8	I/O-B3
11	I/O-A6	I/O-A11	33	I/O-B7	I/O-B2
12	I/O-A7	I/O-A12	34	I/O-B6	I/O-B1
13	I/O-A8	I/OA13	35	V_{CC}	I/O-B0
14	I/O-A9	I/O-A14	36	I/O-B5	GND
15	V_{CC}	I/O-A15	37	I/O-B4	IN0/CK0
16	I/O-A10	GND	38	I/O-B3	IN2-gtsn
17	I/O-A11	V_{CC}	39	I/O-B2	IN1
18	I/O-A12	I/O-B15	40	I/O-B1	IN3
19	I/O-A13	I/O-B14	41	I/O-B0	V_{CC}
20	I/O-A14	I/O-B13	42	GND	I/O-A0-CK3
21	I/O-A15	I/O-B12	43	I/O-CK0	I/O-A1
22	GND	I/O-B11	44	IN2-gtsn	I/O-A2

XCR5032 - 44-pin PLCC



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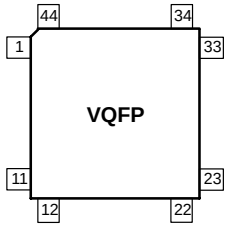
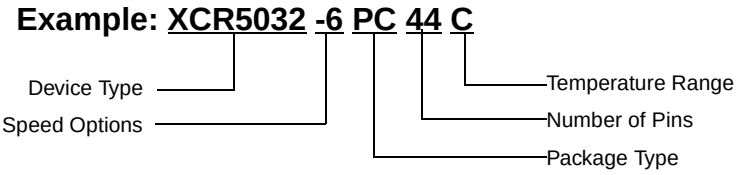
XCR5032 - 44-pin VQFP



SP00433A

Ordering Information



Speed Options
-10: 10 ns pin-to-pin delay
-7: 7.5 ns pin-to-pin delay
-6: 6 ns pin-to-pin delay

Temperature Range
C = Commercial, T_A = 0°C to +70°C
I = Industrial, T_A = –40°C to +85°C

Packaging Options
VQ44: 44-pin VQFP
PC44: 44-pin PLCC

Component Availability

Pins		44	
Type		Plastic VQFP	Plastic PLCC
Code		VQ44	PC44
XCR5032	-10	C, I	C, I
	-7	C, I	C, I
	-6	C	C

Revision History

Date	Version #	Revision
9/15/99	1.0	Initial Xilinx release.
2/10/00	1.1	Converted to Xilinx format and updated.