QPRO™ XQ4000XL Series QML High-Reliability FPGAs

January 4, 1999 (Version 1.1)

XQ4000X Series Features

- Certified to MIL-PRF-38535 Appendix A QML (Qualified Manufacturer Listing)
- Ceramic and plastic packages
- Also available under the following standard microcircuit drawings (SMD)
  - XQ4013XL 5962-98513
  - XQ4036XL 5962-98510
  - XQ4062XL 5962-98511
- For more information contact the Defense Supply Center Columbus (DSCC)
  http://www.dscc.dla.mis/v/va/smd/smdsrch.html
- Available in -3 speed
- System featured Field-Programmable Gate Arrays
  - Select-RAM™ memory: on-chip ultra-fast RAM with
    - synchronous write option
    - dual-port RAM option
  - Abundant flip-flops
  - Flexible function generators
  - Dedicated high-speed carry logic
  - Wide edge decoders on each edge
  - Hierarchy of interconnect lines
  - Internal 3-state bus capability
  - 8 global low-skew clock or signal distribution networks
- System Performance beyond 50 MHz
- Flexible Array Architecture
- Low Power Segmented Routing Architecture
- Systems-Oriented Features
  - IEEE 1149.1-compatible boundary scan logic support
  - Individually programmable output slew rate
  - Programmable input pull-up or pull-down resistors
  - 12-mA Sink Current Per XQ4000XL Output
- Configured by Loading Binary File
  - Unlimited reprogrammability
- Readback Capability
  - Program verification
  - Internal node observability
- Development System runs on most common computer platforms
  - - Interfaces to popular design environments
  - - Fully automatic mapping, placement and routing
  - - Interactive design editor for design optimization
- Highest Capacity — Over 130,000 Usable Gates
- Additional Routing Over XQ4000E
  - almost twice the routing capacity for high-density designs
- Buffered Interconnect for Maximum Speed
- New Latch Capability in Configurable Logic Blocks
- Improved VersaRing™ I/O Interconnect for Better Fixed Pinout Flexibility
  - Virtually unlimited number of clock signals
- Optional Multiplexer or 2-input Function Generator on Device Outputs
- 5V tolerant I/Os
- 0.35m SRAM process

Introduction

XQ4000X Series high-performance, high-capacity Field Programmable Gate Arrays (FPGAs) provide the benefits of custom CMOS VLSI, while avoiding the initial cost, long development cycle, and inherent risk of a conventional masked gate array.

The result of thirteen years of FPGA design experience and feedback from thousands of customers, these FPGAs combine architectural versatility, on-chip Select-RAM memory with edge-triggered and dual-port modes, increased speed, abundant routing resources, and new, sophisticated soft-ware to achieve fully automated implementation of complex, high-density, high-performance designs.

Refer to the complete Commercial XC4000X Series Field Programmable Gate Arrays Data Sheet for more information on device architecture and timing, and the latest Xilinx databook for package pinouts other than the CB228 (included in this data sheet). (Pinouts for XQ4000XL device are identical to XC4000XL.)

Table 1: XQ4000X Series High Reliability Field Progammable Gate Arrays

Device	Logic Cells	Max Logic Gates (No RAM)	Max. RAM Bits (No Logic)	Typical Gate Range (Logic and RAM)*	CLB Matrix	Total CLBs	Number of Flip-Flops	Max. User I/O	Packages
XQ4013XL	2432	13,000	18,432	10,000-30,000	24x24	576	1,536	192	PG223, CB228 PQ240, BG256
XQ4036XL	3078	36,000	41,472	22,000-65,000	36x36	1,296	3,168	288	PG411, CB228, HQ240, BG352
XQ4062XL	5472	62,000	73,728	40,000-130,000	48x48	2,304	5,376	384	PG475, CB228, HQ240, BG432

* Maximum values of typical gate range includes 20% to 30% of CLBs used as RAM.

XQ4000XL Switching Characteristics

Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on preliminary characterization. Further changes are not expected.

Unmarked: Specifications not identified as either Advance or Preliminary are to be considered final.

All specifications subject to change without notice.

Additional Specifications

Except for pin-to-pin input and output parameters, the a.c. parameter delay specifications included in this document are derived from measuring internal test patterns. All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications. For design considerations requiring more detailed timing information, see the appropriate family a.c. supplements available on the Xilinx WEBLINX at http://www.xilinx.com.

Absolute Maximum Ratings

Symbol	Description			Units
V_{CC}	Supply voltage relative to GND		-0.5 to 4.0	V
V_{IN}	Input voltage relative to GND (Note 1)		-0.5 to 5.5	V
V_{TS}	Voltage applied to 3-state output (Note 1)		-0.5 to 5.5	V
V_{CCt}	Longest Supply Voltage Rise Time from 1 V to 3V		50	ms
T_{STG}	Storage temperature (ambient)		-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)		+260	°C
T_J	Junction temperature	Ceramic Package	+150	°C
		Plastic Package	+125	°C

Note 1: Maximum DC overshoot or undershoot above V_{cc} or below GND must be limited to either 0.5 V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to -2.0 V or overshoot to + 7.0 V, provided this over- or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.

Note 2: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}	Supply voltage relative to GND, T_J = -55°C to +125°C	Plastic	3.0	3.6	V
	Supply voltage relative to GND, T_C = -55°C to +125°C	Ceramic	3.0	3.6	V
V_{IH}	High-level input voltage		50% of V_{CC}	5.5	V
V_{IL}	Low-level input voltage		0	30% of V_{CC}	V
T_{IN}	Input signal transition time			250	ns

Note 1: At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per C
Note 2: Input and output measurement threshold is ~50% of V_{CC}.

XQ4000XL DC Characteristics Over Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{OH}	High-level output voltage @ I_{OH} = -4.0 mA, V_{CC} min (LVTTL)		2.4		V
	High-level output voltage @ I_{OH} = -500 µA, (LVCMOS)		90% V_{CC}		V
V_{OL}	Low-level output voltage @ I_{OL} = 12.0 mA, V_{CC} min (LVTTL) (Note 1)			0.4	V
	Low-level output voltage @ I_{OL} = 1500 µA, (LVCMOS)			10% V_{CC}	V
V_{DR}	Data Retention Supply Voltage (below which configuration data may be lost)		2.5		V
I_{CCO}	Quiescent FPGA supply current (Note 2)			5	mA
I_L	Input or output leakage current		-10	+10	µA
C_{IN}	Input capacitance (sample tested)	BGA, PQ, HQ, packages		10	pF
		PGA packages		16	pF
I_{RPU}	Pad pull-up (when selected) @ V_{in} = 0 V (sample tested)		0.02	0.25	mA
I_{RPD}	Pad pull-down (when selected) @ V_{in} = 3.6 V (sample tested)		0.02	0.15	mA
I_{RLL}	Horizontal Longline pull-up (when selected) @ logic Low		0.3	2.0	mA

Note 1: With up to 64 pins simultaneously sinking 12 mA.
Note 2: With no output current loads, no active input or Longline pull-up resistors, all I/O pins Tri-stated and floating.

XQ4000XL Global Buffer Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

When fewer vertical clock lines are connected, the clock distribution is faster; when multiple clock lines per column are driven from the same global clock, the delay is longer. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

		Speed Grade	-3	Units
Description	**Symbol**	**Device**	**Max**	
From pad through Global Low Skew buffer, to any clock K	T_{GLS}	XQ4013XL XQ4036XL XQ4062XL	3.6 4.8 6.3	ns ns ns
From pad through Global Early buffer, to any IOB clockK. Values are for BUFGE #s 1, 2, 5 and 6. Add 1 - 2 ns for BUFGE #s 3, 4, 7 and 8 and for all CLB clock Ks driven from any of the 8 BUFGEs, or consult TRCE.	T_{GE}	XQ4013XL XQ4036XL XQ4062XL	2.4 3.1 4.9	ns ns ns

XQ4000XL CLB Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQ4000XL devices and expressed in nanoseconds unless otherwise noted.

	Speed Grade	-3		Units
Description	**Symbol**	**Min**	**Max**	
Combinatorial Delays				
F/G inputs to X/Y outputs	T_{ILO}		1.6	ns
F/G inputs via H' to X/Y outputs	T_{IHO}		2.7	ns
F/G inputs via transparent latch to Q outputs	T_{ITO}		2.9	ns
C inputs via SR/H0 via H to X/Y outputs	T_{HH0O}		2.5	ns
C inputs via H1 via H to X/Y outputs	T_{HH1O}		2.4	ns
C inputs via DIN/H2 via H to X/Y outputs	T_{HH2O}		2.5	ns
C inputs via EC, DIN/H2 to YQ, XQ output (bypass)	T_{CBYP}		1.5	ns
CLB Fast Carry Logic				
Operand inputs (F1, F2, G1, G4) to C_{OUT}	T_{OPCY}		2.7	ns
Add/Subtract input (F3) to C_{OUT}	T_{ASCY}		3.3	ns
Initialization inputs (F1, F3) to C_{OUT}	T_{INCY}		2.0	ns
C_{IN} through function generators to X/Y outputs	T_{SUM}		2.8	ns
C_{IN} to C_{OUT}, bypass function generators	T_{BYP}		0.26	ns
Carry Net Delay, C_{OUT} to C_{IN}	T_{NET}		0.32	ns
Sequential Delays				
Clock K to Flip-Flop outputs Q	T_{CKO}		2.1	ns
Clock K to Latch outputs Q	T_{CKLO}		2.1	ns
Setup Time before Clock K				
F/G inputs	T_{ICK}	1.1		ns
F/G inputs via H	T_{IHCK}	2.2		ns
C inputs via H0 through H	T_{HH0CK}	2.0		ns
C inputs via H1 through H	T_{HH1CK}	1.9		ns
C inputs via H2 through H	T_{HH2CK}	2.0		ns
C inputs via DIN	T_{DICK}	0.9		ns
C inputs via EC	T_{ECCK}	1.0		ns
C inputs via S/R, going Low (inactive)	T_{RCK}	0.6		ns
CIN input via F/G	T_{CCK}	2.3		ns
CIN input via F/G and H	T_{CHCK}	3.4		ns
Hold Time after Clock K				
F/G inputs	T_{CKI}	0		ns
F/G inputs via H	T_{CKIH}	0		ns
C inputs via SR/H0 through H	T_{CKHH0}	0		ns
C inputs via H1 through H	T_{CKHH1}	0		ns
C inputs via DIN/H2 through H	T_{CKHH2}	0		ns
C inputs via DIN/H2	T_{CKDI}	0		ns
C inputs via EC	T_{CKEC}	0		ns
C inputs via SR, going Low (inactive)	T_{CKR}	0		ns
Clock				
Clock High time	T_{CH}	3.0		ns
Clock Low time	T_{CL}	3.0		ns
Set/Reset Direct				
Width (High)	T_{RPW}	3.0		ns
Delay from C inputs via S/R, going High to Q	T_{RIO}		3.7	ns
Global Set/Reset				
Minimum GSR Pulse Width	T_{MRW}		19.8	ns
Delay from GSR input to any Q	T_{MRQ}	See page 66 for T_{RRI} values per device.		
Toggle Frequency (MHz) (for export control)	F_{TOG}		166	MHz

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XQ4000XL RAM Synchronous (Edge-Triggered) Write Operation Guidelines

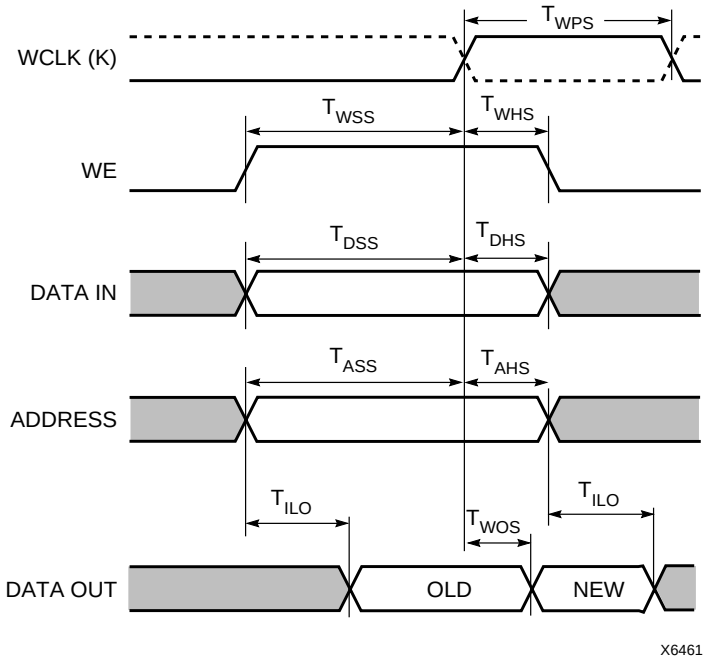
Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQ4000XL devices and are expressed in nanoseconds unless otherwise noted.

Single Port RAM	**Speed Grade**		**-3**		**Units**
	Size	**Symbol**	**Min**	**Max**	
Write Operation					
Address write cycle time (clock K period)	16x2 32x1	T_{WCS} T_{WCTS}	9.0 9.0		ns ns
Clock K pulse width (active edge)	16x2 32x1	T_{WPS} T_{WPTS}	4.5 4.5		ns ns
Address setup time before clock K	16x2 32x1	T_{ASS} T_{ASTS}	2.2 2.2		ns ns
Address hold time after clock K	16x2 32x1	T_{AHS} T_{AHTS}	0 0		ns ns
DIN setup time before clock K	16x2 32x1	T_{DSS} T_{DSTS}	2.0 2.5		ns ns
DIN hold time after clock K	16x2 32x1	T_{DHS} T_{DHTS}	0 0		ns ns
WE setup time before clock K	16x2 32x1	T_{WSS} T_{WSTS}	2.0 1.8		ns ns
WE hold time after clock K	16x2 32x1	T_{WHS} T_{WHTS}	0 0		ns ns
Data valid after clock K	16x2 32x1	T_{WOS} T_{WOTS}		6.8 8.1	ns ns
R**ead Operation**					
Address read cycle time	16x2 32x1	T_{RC} T_{RCT}	4.5 6.5		ns ns
Data Valid after address change (no Write Enable)	16x2 32x1	T_{ILO} T_{IHO}		1.6 2.7	ns ns
Address setup time before clock K	16x2 32x1	T_{ICK} T_{IHCK}	1.3 2.3		ns ns

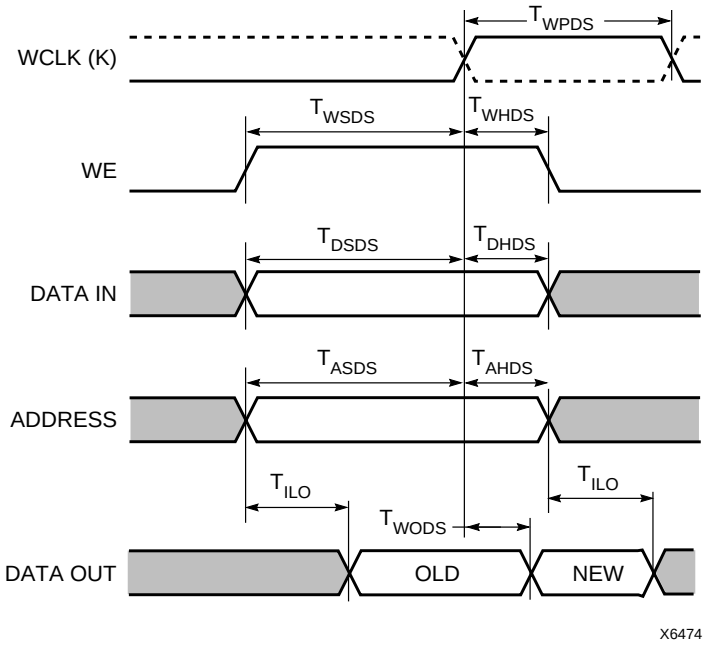
Dual Port RAM	Speed Grade		-3		Units
	Size	Symbol	Min	Max	
Write Operation					
Address write cycle time (clock K period)	16x1	T_{WCDS}	9.0		ns
Clock K pulse width (active edge)	16x1	T_{WPDS}	4.5		ns
Address setup time before clock K	16x1	T_{ASDS}	2.5		ns
Address hold time after clock K	16x1	T_{AHDS}	0		ns
DIN setup time before clock K	16x1	T_{DSDS}	2.5		ns
DIN hold time after clock K	16x1	T_{DHDS}	0		ns
WE setup time before clock K	16x1	T_{WSDS}	1.8		ns
WE hold time after clock K	16x1	T_{WHDS}	0		ns
Data valid after clock K	16x1	T_{WODS}		7.8	ns

Note 1: Timing for16 x1 RAM option is identical to16 x 2 RAM.

XQ4000XL CLB RAM Synchronous (Edge-Triggered) Write Timing



XQ4000XL CLB Dual-Port RAM Synchronous (Edge-Triggered) Write Timing



XQ4000XL Pin-to-Pin Output Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values are expressed in nanoseconds unless otherwise noted.

XQ4000XL Output Flip-Flop, Clock to Out

		Speed Grade	-3	Units
Description	**Symbol**	**Device**	**Max**	
Global Low Skew Clock to Output using OFF	T_{ICKOF}	XQ4013XL XQ4036XL XQ4062XL	8.6 9.8 11.3	ns ns ns
Global Early Clock to Output using OFF Values are for BUFGE #s 3, 4, 7, and 8. Add 1.4 ns for BUFGE #s 1, 2, 5, and 6.	T_{ICKEOF}	XQ4013XL XQ4036XL XQ4062XL	7.4 8.1 9.9	ns ns ns
For output SLOW option add	T_{SLOW}	All Devices	3.0	ns

OFF = Output Flip Flop

Note 1: Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
Note 2: Output timing is measured at ~50% V_{CC} threshold with 50 pF external capacitive load. For different loads, see graph below.

XQ4000XL Output Mux, Clock to Out

		Speed Grade	-3	Units
Description	**Symbol**	**Device**	**Max**	
Global Low Skew Clock to Output using OFF	T_{ICKOF}	XQ4013XL XQ4036XL XQ4062XL	8.8 10.0 11.4	ns ns ns
Global Early Clock to Output using OFF. Values are for BUFGE #s 3, 4, 7, and 8. Add 1.4 ns for BUFGE #s 1, 2, 5, and 6.	T_{ICKEOF}	XQ4013XL XQ4036XL XQ4062XL	7.6 8.2 10.0	ns ns ns
For output SLOW option add	T_{SLOW}	All Devices	3.0	ns

OFF = Output Flip Flop

Note 1: Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
Note 2: Output timing is measured at ~50% V_{CC} threshold with 50 pF external capacitive load. For different loads, see graph below.

Capacitive Load Factor

Figure 1 shows the relationship between I/O output delay and load capacitance. It allows a user to adjust the specified output delay if the load capacitance is different than 50 pF. For example, if the actual load capacitance is 120 pF, add 2.5 ns to the specified delay. If the load capacitance is 20 pF, subtract 0.8 ns from the specified output delay.

Figure 1 is usable over the specified operating conditions of voltage and temperature and is independent of the output slew rate control.

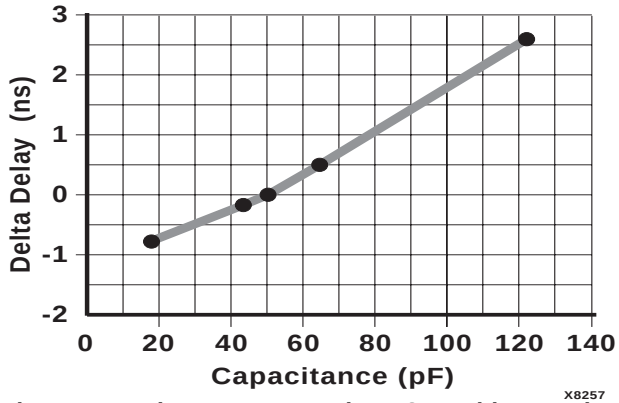


Figure 1: Delay Factor at Various Capacitive Loads

XQ4000XL Pin-to-Pin Input Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values are expressed in nanoseconds unless otherwise noted.

XQ4000XL Global Low Skew Clock, Set-Up and Hold

		Speed Grade	-3	Units
Description	**Symbol**	**Device**	**Min**	
Input Setup and Hold Times Using Global Low Skew Clock and IFF				
No Delay	T_{PSN}/T_{PHN}	XQ4013XL	1.2 / 3.2	ns
		XQ4036XL	1.2 / 5.5	ns
		XQ4062XL	1.2 / 7.0	ns
Partial Delay	T_{PSP}/T_{PHP}	XQ4013XL	6.1 / 0.0	ns
		XQ4036XL	6.4 / 1.0	ns
		XQ4062XL	6.7 / 1.2	ns
Full Delay	T_{PSD}/T_{PHD}	XQ4013XL	6.4 / 0.0	ns
		XQ4036XL	6. 6 / 0.0	ns
		XQ4062XL	6.8 / 0.0	ns

IFF = Input Flip-Flop or Latch

Note 1: Setup time is measured with the fastest route and the lightest load. Hold time is measured using the furthest distance and a reference load of one clock pin per two IOBs. Use the static timing analyzer (TRCE) to determine the setup and hold times under given design conditions.

XQ4000XL BUFGE #s 3, 4, 7, & 8 Global Early Clock, Set-up and Hold for IFF and FCL

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values are expressed in nanoseconds unless otherwise noted.

		Speed Grade	-3
Description	**Symbol**	**Device**	**Min**
Input Setup and Hold Times			
No Delay		XQ4013XL	1.2 / 4.7
Global Early Clock and IFF	T_{PSEN}/T_{PHEN}	XQ4036XL	1.2 / 6.7
Global Early Clock and FCL	T_{PFSEN}/T_{PFHEN}	XQ4062XL	1.2 / 8.4
Partial Delay		XQ4013XL	5.4 / 0.0
Global Early Clock and IFF	T_{PSEP}/T_{PHEP}	XQ4036XL	6.4 / 0.8
Global Early Clock and FCL	T_{PFSEP}/T_{PFHEP}	XQ4062XL	8.4 / 1.5
Full Delay		XQ4013XL	12.0 / 0.0
Global Early Clock and IFF	T_{PSED}/T_{PHED}	XQ4036XL	13.8 / 0.0
		XQ4062XL	13.1 / 0.0

IFF = Input Flip-Flop or Latch, FCL = Fast Capture Latch

Note 1: Setup time is measured with the fastest route and the lightest load. Hold time is measured using the furthest distance and a reference load of one clock pin per two IOBs. Use the static timing analyzer(TRCE) to determine the setup and hold times under given design conditions.

XQ4000XL BUFGE #s 1, 2, 5, & 6 Global Early Clock, Set-up and Hold for IFF and FCL

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values are expressed in nanoseconds unless otherwise noted.

		Speed Grade	-3
Description	**Symbol**	**Device**	**Min**
Input Setup and Hold Times			
No Delay		XQ4013XL	1.2 / 4.7
Global Early Clock and IFF	T_{PSEN}/T_{PHEN}	XQ4036XL	1.2 / 6.7
Global Early Clock and FCL	T_{PFSEN}/T_{PFHEN}	XQ4062XL	1.2 / 8.4
Partial Delay		XQ4013XL	6.4 / 0.0
Global Early Clock and IFF	T_{PSEP}/T_{PHEP}	XQ4036XL	7.0 / 0.0
Global Early Clock and FCL	T_{PFSEP}/T_{PFHEP}	XQ4062XL	9.0 / 0.8
Full Delay		XQ4013XL	10.0 / 0.0
Global Early Clock and IFF	T_{PSED}/T_{PHED}	XQ4036XL	12.2 / 0.0
		XQ4062XL	13.1 / 0.0

IFF = Input Flip-Flop or Latch, FCL = Fast Capture Latch

Note 1: Setup time is measured with the fastest route and the lightest load. Hold time is measured using the furthest distance and a reference load of one clock pin per two IOBs. Use the static timing analyzer(TRCE) to determine the setup and hold times under given design conditions.

XQ4000XL IOB Input Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

		Speed Grade	-3	Units
Description	**Symbol**	**Device**	**Min**	
Clocks				
Clock Enable (EC) to Clock (IK)	T_{ECIK}	All devices	0.3	ns
Delay from FCL enable (OK) active edge to IFF clock (IK) active edge	T_{OKIK}	All devices	1.7	ns
Setup Times				
Pad to Clock (IK), no delay	T_{PICK}	All devices	1.7	ns
Pad to Clock (IK), via transparent Fast Capture Latch, no delay	T_{PICKF}	All devices	2.3	ns
Pad to Fast Capture Latch Enable (OK), no delay	T_{POCK}	All devices	0.7	ns
Hold Times				
All Hold Times		All devices	0	ns
Global Set/Reset				
Minimum GSR Pulse Width	T_{MRW}	All devices	19.8	ns
Delay from GSR input to any Q	T_{RRI}	XQ4013XL	15.9	ns
		XQ4036XL	22.5	ns
		XQ4062XL	29.1	ns
Propagation Delays			**Max**	
Pad to I1, I2	T_{PID}	All devices	1.6	ns
Pad to I1, I2 via transparent input latch, no delay	T_{PLI}	All devices	2.6	ns
Pad to I1, I2 via transparent FCL and input latch, no delay	T_{PFLI}	All devices	3.1	ns
Clock (IK) to I1, I2 (flip-flop)	T_{IKRI}	All devices	1.8	ns
Clock (IK) to I1, I2 (latch enable, active Low)	T_{IKLI}	All devices	1.9	ns
FCL Enable (OK) active edge to I1, I2 (via transparent standard input latch)	T_{OKLI}	All devices	3.6	ns

IFF = Input Flip-Flop or Latch, FCL = Fast Capture Latch

XQ4000XL IOB Output Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). For Propagation Delays, slew-rate = fast unless otherwise noted. Values are expressed in nanoseconds unless otherwise noted.

		-3		Units
Description	**Symbol**	**Min**	**Max**	
Clocks				
Clock High	T_{CH}	3.0		ns
Clock Low	T_{CL}	3.0		ns
Propagation Delays				
Clock (OK) to Pad	T_{OKPOF}		5.0	ns
Output (O) to Pad	T_{OPF}		4.1	ns
3-state to Pad hi-Z (slew-rate independent)	T_{TSHZ}		4.4	ns
3-state to Pad active and valid	T_{TSONF}		4.1	ns
Output (O) to Pad via Fast Output MUX	T_{OFPF}		5.5	ns
Select (OK) to Pad via Fast MUX	T_{OKFPF}		5.1	ns
Setup and Hold Times				
Output (O) to clock (OK) setup time	T_{OOK}	0.5		ns
Output (O) to clock (OK) hold time	T_{OKO}	0.0		ns
Clock Enable (EC) to clock (OK) setup time	T_{ECOK}	0.0		ns
Clock Enable (EC) to clock (OK) hold time	T_{OKEC}	0.3		ns
Global Set/Reset				
Minimum GSR pulse width	T_{MRW}	19.8		ns
Delay from GSR input to any Pad	T_{RPO}			
XQ4013XL		20.5		ns
XQ4036XL		27.1		ns
XQ4062XL		33.7		ns
Slew Rate Adjustment				
For output SLOW option add	T_{SLOW}		3.0	ns

Note 1: Output timing is measured at ~50% V_{CC} threshold, with 50 pF external capacitive loads.

Pinouts

CB228 Package for XQ4013XL/4036XL/4062XL

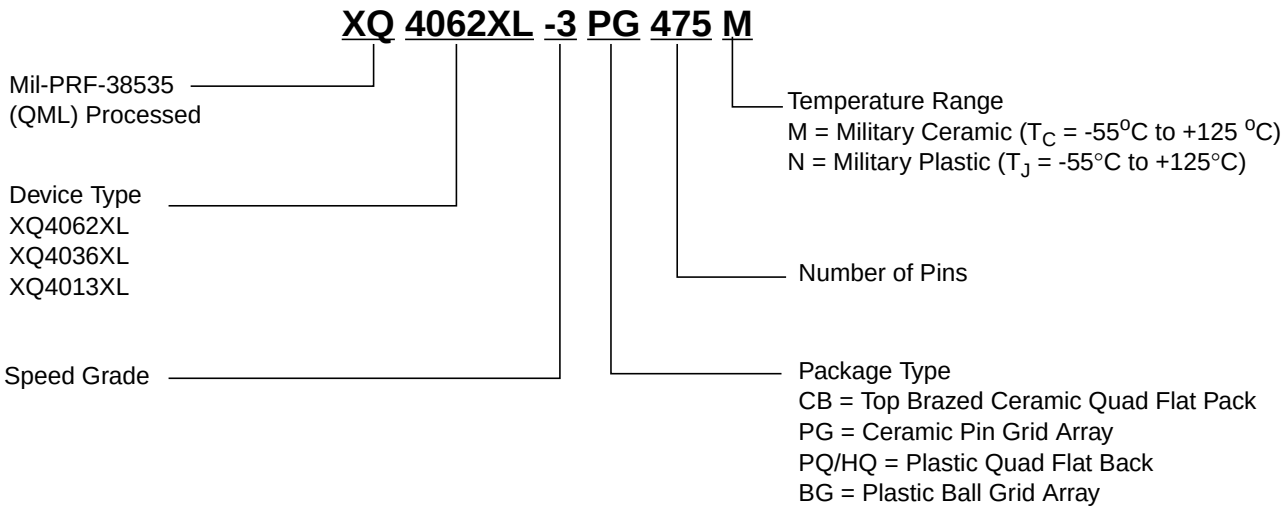
PIN_NAME	CB228
VTT	
VSS	P1
BUFGP_TL_A16_GCK1_IO	P2
A17_IO	P3
IO	P4
IO	P5
TDI_IO	P6
TCK_IO	P7
IO	P8
IO	P9
IO	P10
IO	P11
IO	P12
IO	P13
VSS	P14
IO_FCLK1	P15
IO	P16
TMS_IO	P17
IO	P18
IO	P19
IO	P20
IO	P21
IO	P22
IO	P23
IO	P24
IO	P25
IO	P26
VSS	P27
VCC	P28
IO	P29
IO	P30
IO	P31
IO	P32
IO	P33
IO	P34
IO	P35
IO	P36
VCC	P37
IO	P38
IO	P39
IO	P40
IO_FCLK2	P41
VSS	P42
IO	P43
IO	P44
IO	P45
IO	P46
IO	P47
IO	P48
IO	P49
IO	P50
IO	P51
IO	P52
IO	P53
BUFGS_BL_GCK2_IO	P54
M1	P55
VSS	P56
M0	P57
VCC	P58
M2	P59
BUFGP_BL_GCK3_IO	P60
HDC_IO	P61
IO	P62
IO	P63
IO	P64
LDC_IO	P65
IO	P66
IO	P67
IO	P68
IO	P69
IO	P70
IO	P71
VSS	P72
IO	P73
IO	P74
IO	P75
IO	P76
IO	P77
IO	P78
IO	P79
IO	P80
IO	P81
IO	P82
IO	P83
/ERR_INIT_IO	P84
VCC	P85
VSS	P86
IO	P87
IO	P88

PIN_NAME	CB228
IO	P89
IO	P90
IO	P91
IO	P92
IO	P93
IO	P94
VCC	P95
IO	P96
IO	P97
IO	P98
IO	P99
VSS	P100
IO	P101
IO	P102
IO	P103
IO	P104
IO	P105
IO	P106
IO	P107
IO	P108
IO	P109
IO	P110
IO	P111
BUFGS_BR_GCK4_IO	P112
VSS	P113
DONE	P114
VCC	P115
/PROG	P116
D7_IO	P117
BUFGP_BR_GCK5_IO	P118
IO	P119
IO	P120
IO	P121
IO	P122
D6_IO	P123
IO	P124
IO	P125
IO	P126
IO	P127
IO	P128
VSS	P129
IO	P130
IO	P131
IO_FCLK3	P132
IO	P133
D5_IO	P134
/CS0_IO	P135
IO	P136

PIN_NAME	CB228
IO	P137
IO	P138
IO	P139
D4_IO	P140
IO	P141
VCC	P142
VSS	P143
D3_IO	P144
/RS_IO	P145
IO	P146
IO	P147
IO	P148
IO	P149
D2_IO	P150
IO	P151
VCC	P152
IO	P153
IO_FCLK4	P154
IO	P155
IO	P156
VSS	P157
IO	P158
IO	P159
IO	P160
IO	P161
IO	P162
IO	P163
D1_IO	P164
BUSY_/RDY_RCLK_IO	P165
IO	P166
IO	P167
D0_DIN_IO	P168
BUFGS_TR_GCK6_DOUT_IO	P169
CCLK	P170
VCC	P171
TDO	P172
VSS	P173
A0_/WS_IO	P174
BUFGP_TR_GCK7_A1_IO	P175
IO	P176
IO	P177
CSI_A2_IO	P178
A3_IO	P179
IO	P180
IO	P181
IO	P182
IO	P183
IO	P184

PIN_NAME	CB228
IO	P185
VSS	P186
IO	P187
IO	P188
IO	P189
IO	P190
VCC	P191
A4_IO	P192
A5_IO	P193
IO	P194
IO	P195
A21_IO	P196
A20_IO	P197
A6_IO	P198
A7_IO	P199
VSS	P200
VCC	P201
A8_IO	P202
A9_IO	P203
A19_IO	P204
A18_IO	P205
IO	P206
IO	P207
A10_IO	P208
A11_IO	P209
VCC	P210
IO	P211
IO	P212
IO	P213
IO	P214
VSS	P215
IO	P216
IO	P217
IO	P218
IO	P219
A12_IO	P220
A13_IO	P221
IO	P222
IO	P223
IO	P224
IO	P225
A14_IO	P226
BUFGS_TL_GCK8_A15_IO	P227
VCC	P228

Ordering Information



Revision History

Date	Version	Description
5/98	1.0	Original document release.
12/98	1.1	Addition of new packages, clarification of parameters.