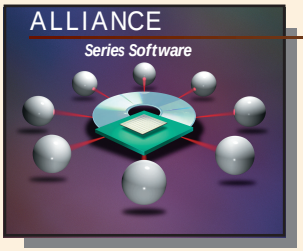

Exemplar Information

Device Architecture Support

FPGA	XC3000(A, L)	XC4000(E, L)
	XC4000(EX, XL, XV, XLA)	XC5000
	Virtex	XC9000
	Spartan	XC9000XL
	Spartan-XL	
CPLD	XC9500 and XC9500XL	

Recommended Settings

For recommended settings, go to
http://www.xilinx.com
"Product"→"Software Solutions"

Xilinx Contacts and Technical Support

World Wide Web:
http://www.xilinx.com

North America
1-800-255-7778
hotline@xilinx.com

France
33 1-3463-0100
frhelp@xilinx.com

United Kingdom
44 1932-820821
ukhelp@xilinx.com

Japan
81 3-3297-9163
jhotline@xilinx.com

Exemplar Contacts and Technical Support

World Wide Web:
http://www.exemplar.com
Tom Hill, Xilinx Relationship Manager
1-503-685-7750
Hoa Dina, Technical Support Manager
1-510-337-3700

HDL Library and Language Support

HDL Libraries meet all the HDL Standards
IEEE 1076, -87, & -93, IEEE 1164 VHDL OVI 2.0 and Verilog-XL
Libraries include: • **std_logic_1164**
• **std_logic_arith** • **std_logic_signed**
• **std_logic_unsigned** • **attributes**

Guide Overview

1 Invoke the tools

Galileo

PC	**start→Galileo Vx→Galileo**
UNIX	**Galileo**

Leonardo

PC	**start→leonardo Vx→leonardo** **start→leonardo Vx→lgalileo license**
UNIX	**leonardo**

2 Specify input files

Galileo •Select file name in input design

Leonardo •Run flow guide after selecting the target technology
•A new window called leonardo flow guide
•Read <input file> select file

3 Select target architecture

Galileo • Under **Output Design**→choose **Technology**

Leonardo • Flow Guide prompts for technology select **Target Technology**

4 Synthesis Commands

Timing constraints are specified in the constraint file. Please refer to the online documentation for information on how to specify constraints.

5 Synthesize

To synthesize press **start run** button