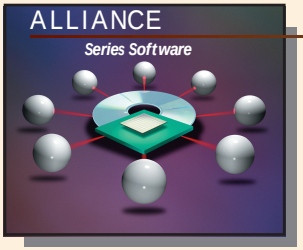

Synopsys FPGA Express Information

Device Architecture Support

FPGA	XC3000(A, L)	XC4000(E, L)
	XC4000(EX, XL, XV, XLA)	XC5000
	Virtex	XC9000
	Spartan	XC9000XL
	Spartan-XL	
CPLD	XC9500 and XC9500XL	

Recommended Settings

Please refer to your A1.5 software installation and the examples:
.synopsys_dc.setup
.synopsys_vss.setup
and the runscript files in
$XILINX/synopsys/examples

Xilinx Contacts and Technical Support

World Wide Web:
http://www.xilinx.com

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United Kingdom
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33 1-3463-0100
frhelp@xilinx.com
Japan
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jhotline@xilinx.com

Synopsys Contacts and Technical Support

World Wide Web:
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United States
1-800-245-8005
support_center@synopsys.com

Guide Overview

1 Create a project

Go to menu **File→New** and define a new project. All HDL files processed by FPGA Express must be done through a project.

2 Add HDL files to project and analyze HDL files

After creating project, HDL design files can be added to the project. After adding the HDL design files, **FPGA *Express*** will automatically analyze the HDL files.

3 Implement the design

Select the top-level **module/entity** in the **Design Sources** window and the **implement** button will be highlighted.
Click on the implement button and specify the target **die**, **speed grade** and **package**.
Strategies for synthesis can be specified during implementation.

4 Enter constraints

In the **Chips** window, **select the implementation**. Right-click on the selected implementation and select **Edit Constraints**. A window will appear where various constraints can be edited.
After entering constraints, save constraints by **closing the constraints window.**

5 Optimize the design

Click on the **optimize** button located next to the implement button to synthesize the design OR select the menu **Synthesis→Optimize Chip**

6 Place&Route an XNF file with A1.5

After optimization, write out the XNF file by clicking on the **Export Netlist** button next to the implement button. **Place and Route** the XNF file using **A1.5 implementation tools** with the Design Manager GUI or DOS shell based commands.

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