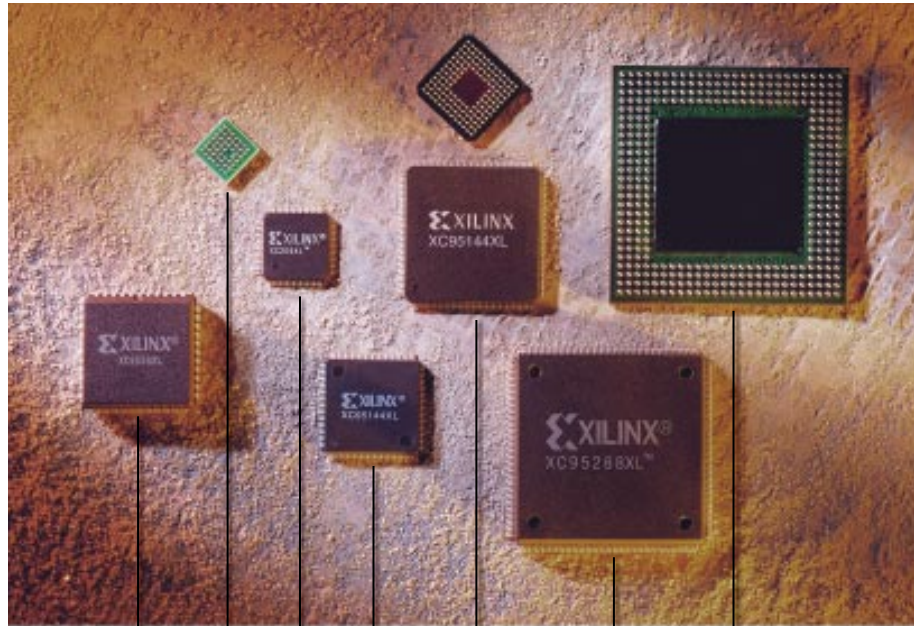# FastFLASH™ CPLD Family

XC9500XL

3.3V, Faster, Lower Power, Lower Cost, New Features

Our new FastFLASH XC9500XL CPLDs expand the capability of our popular XC9500 family, bringing you more speed, more new features, and lower costs, in a new power-saving 3.3V technology. Targeted for leading-edge systems that require rapid design development, longer system life, and robust field upgrade capability, this CPLD family provides unparalleled performance along with the highest programming reliability and ease-of-use. In addition, XC9500XL CPLDs easily complement our higher density FPGAs, giving you a total, seamless, logic solution; a robust, unified development environment that makes it very quick and easy for you to translate your creative ideas into working designs.

The tired, old, EEPROM-based CPLD architectures of the past will just get in your way. Let your creativity soar, with the most advanced CPLDs available anywhere – the Xilinx XC9500XL family.

Actual size shown

| 44-Pin PLCC | 48-Pin CSP | 64-Pin VQFP | 100-Pin TQFP | 144-Pin CSP TQFP | 208-Pin PQFP | 256-Pin BGA |

Ideal Applications:

- DRAM controller
- Microprocessor interface
- Video clock generator
- Display driver
- Bus transceiver
- Gate array patch
- PAL/GAL consolidation
- Obsolete LSI replacement

Family Overview:

- 36 to 288 macrocells
- 4ns pin-to-pin speeds with 200MHz system frequency
- Fast in-system programming and erase times
- Superior pin-locking for reliable field upgrade capability
- Full IEEE 1149.1 (JTAG) ISP and boundary-scan test
- 3rd generation, proven, FastFLASH CPLD technology
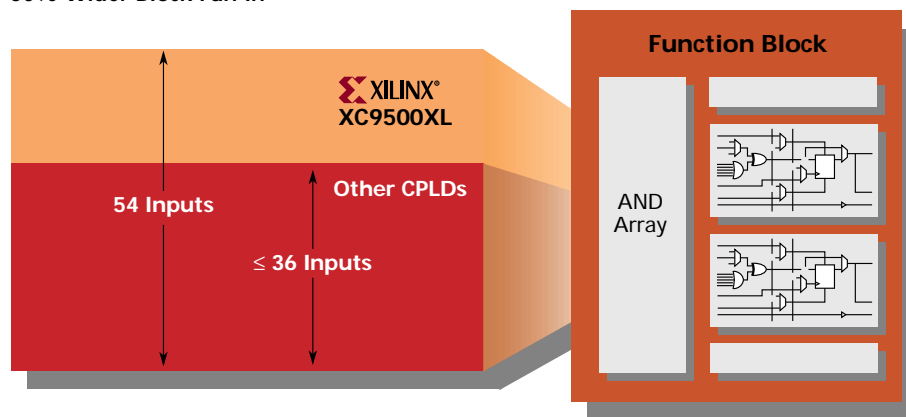
FastFLASH XC9500XL Family

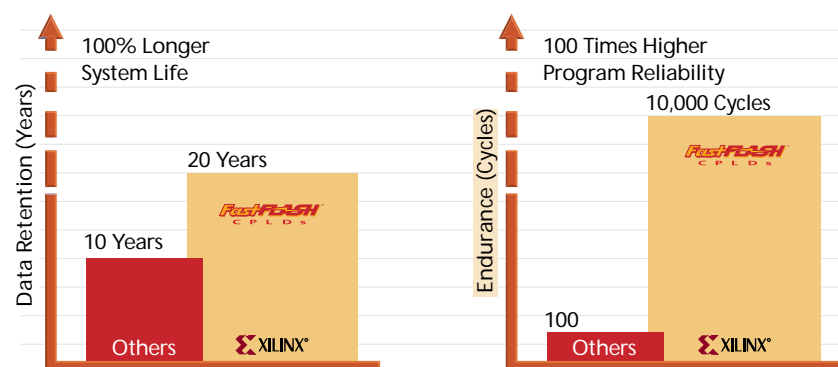|	XC9536XL	XC9572XL	XC95144XL	XC95288XL
Macrocells	36	72	144	288
Usable Gates	800	1,600	3,200	6,400
Registers	36	72	144	288
t_{PD} (ns)	4	5	5	6
f_{SYSTEM} (MHz)	200	178	178	151
User I/O Pins				
44-pin PLCC	34	34		
64-pin VQFP	36	52		
100-pin TQFP		72	81	
144-pin TQFP			117	117
208-pin PQFP				168
48-pin CSP	36	38		
144-pin CSP			117	
256-pin BGA				192

XILINX®

Advanced Architecture

- Ultra-wide 54 input function blocks for fast wide logic
- Oversized 18 macrocell blocks for lookahead logic
- 90 possible product-terms per macrocell
- Three global clocks and product-term clock, with inversion at macrocell
- Global and individual OE per output, with inversion at the output
- Bus-hold circuitry on all user I/O pins
- Input hysteresis on all user and JTAG inputs

50% Wider Block Fan-In

XILINX
XC9500XL

54 Inputs

Other CPLDs
≤ 36 Inputs

Function Block

AND Array

Highest Device Reliability

100% Longer System Life

Data Retention (Years)

10 Years — Others

20 Years — FastFLASH CPLDs / XILINX

100 Times Higher Program Reliability

Endurance (Cycles)

10,000 Cycles — FastFLASH CPLDs / XILINX

100 — Others

Solid Reliability

- Endurance rating of 10,000 cycles
- Virtually eliminates programming failures
- Data retention rating of 20 years
- Supports longer system life
- Immune from "ISP Lock-Out" failure mode
- Allows arbitrary mixed power sequencing ("hot-socketing")

Instant Design Evaluation Via WWW

Fast and easy evaluation for your CPLD designs is available instantly on the Internet. Simply go to the Xilinx homepage (www.xilinx.com) to access the WebFitter software and submit your sample designs. Or contact your local Xilinx sales representative for more information.

Features	Benefits
• Highest performance 4 ns / 200 MHz	• Leading-edge computing applications
• Most flexible pin-locking architecture	• Design iterations without board rework
• Highest device reliability	• Higher quality, reduced support cost
• Smallest packages (CSP)	• Reduced board area, increased flexibility
• In-system programming via JTAG	• Compatible with industry-standard ISP
• Robust 5V, 3.3V, 2.5V interfacing	• Worry-free mixed voltage operation
• 3rd generation FastFLASH process	• Fast programming, rapid cost reduction

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XILINX
The Programmable Logic Company℠