Timing Correction for Flight Time Compensation

With the HyperLynx signal integrity simulation software, you can easily verify the overall timing of your high performance designs.

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As signal and clock speeds increase, and driver edge rates decrease, the routing segments on a printed circuit board become transmission lines. Today, the routing on the board may contribute more to the delay than does the capacitance of the receiver IC. Therefore, modeling the load as a fixed capacitance does not provide good delay prediction on a printed circuit board or multi-chip module. In addition, I/O buffers and logic delays are often modeled and simulated separately, making it difficult for you to create a consistent timing model.

You must correct the fixed timing delays (obtained from the data book) to get the actual values after layout is complete, because the flight time of the signal down the routed nets is usually comparable to the delay through the integrated circuits. Once you have compensated for this "flight time," you can verify timing constraints such as setup and hold times. The compensation calculation starts with the data book delay under fixed loading conditions, and then arrives at a corrected delay for the actual board load (including the wire routing and the receiver) by using signal integrity simulation software such as HyperLynx.

Timing Correction on PC Boards

Integrated circuit (IC) delays presented in data books are specified at a fixed test load, which is selected by the manufacturer as representative of loading for nets with moderate to high fanout and no wires. The data book delay includes both the logic delays and the delay through the I/O driver. On the other hand, I/O buffers are usually modeled using IBIS (I/O Buffer Information Specification) for simulation. In an IBIS model, only the buffer is represented, and there is no information about any logic delays inside the integrated circuit. Fortunately, the IBIS model provides an easy method to compensate board-level delays for flight time effects.

Figure 1 shows the delay between a driver and a receiver for three different loads:

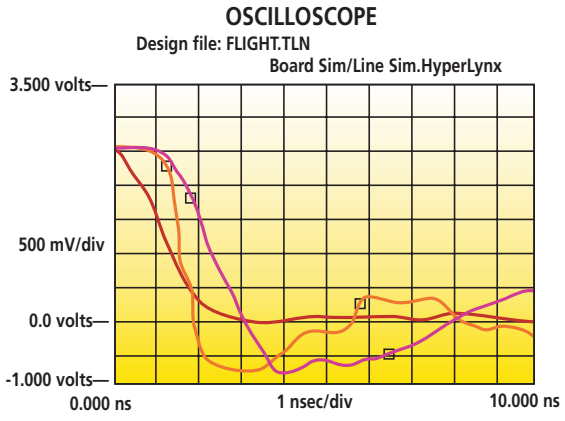

Figure 1: Comparison of delays with loads of (a) 35 pF CREF, (b) 6.5 pF receiver, 6" (11 pF, 68 nH) transmission line and 17.5 pF load capacitor to total 35 pF, (c) 6.5 pF receiver and 6" transmission line.

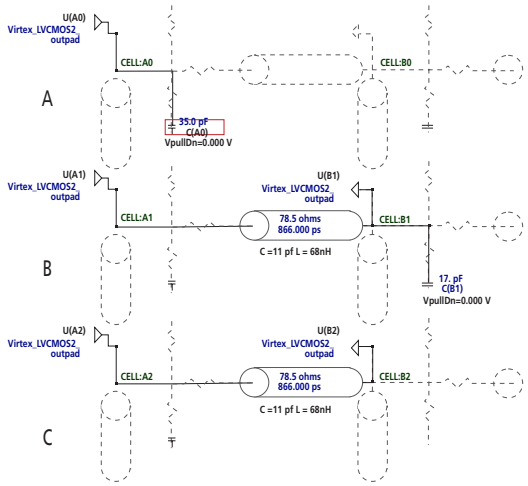

Figure 1.1 - Loading Diagram

(A) The CREF 35pF capacitive load (left curve).

(B) A 6.5 pF receiver, with a 6" transmission line (11 pF), and a 17.5 pF capacitor for a total load of 35 pF (right curve).

(C) Just the 6.5 pF receiver and 6" transmission line (center curve).

The IBIS models used here are for a Xilinx Virtex LVCMOS I/O buffer. This is a dramatic illustration of the effects of transmission line delays being comparable to capacitive loading delays.

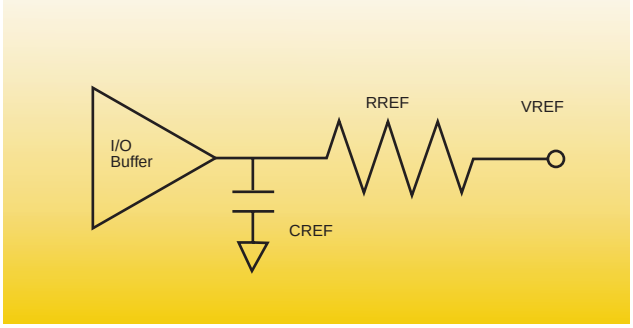

Figure 2 - The IBIS timing model.

The Data Book Delay

The delay presented in a typical data book is from an input (such as CLK or A0) to the output (such as Q or Y2) of an FPGA or other IC. This delay includes two effects: the delay through the IC between the specified input and the input of the I/O buffer, and the time for the I/O buffer to pull the load up (or down) to the manufacturing test voltage VMEAS. This test load may be any combination of CREF and RREF, as shown in Figure 2. The manufacturer assumes that the board-level user will then start any timing measurements from VMEAS.

The data book delays are measured with lumped loads to make manufacturing testing easier. However, on a real printed circuit board or multi-chip module, each routing segment is actually a transmission line—a distributed LC component, as shown in Figure 3. On the typical PC board, the inductance contributes

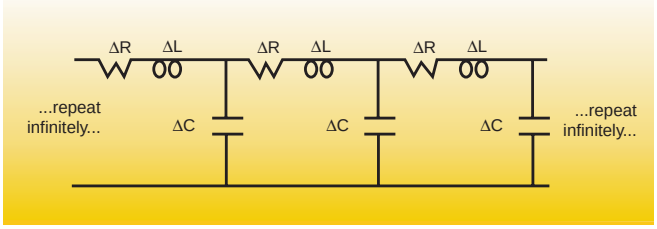

Figure 3 - Electrical model of a transmission line.

significantly to the delay. On a PC board or multi-chip module, for example, the driver and receiver pins may be an inch or more apart. While an inch may not seem like much at first glance, it represents a delay of roughly 200 ps—comparable to the transition time of a fast driver. Therefore, transmission line delays must also be included in timing analysis, even though they are not in the data book delay specifications.

Timing Correction Factors

Figure 4 shows the sequence of events. At T=0, the input changes on the driver IC. At the data book load CREF, TCREF is when the signal has gone through the IC's logic path and the output driver voltage crosses VMEAS. Finally, Tr_max is when the receiver is guaranteed to have changed state. Note that the total delay (Tr_max) may be either positive or negative; this is caused by the manufacturer's choice of CREF and the slew rate of the input signal.

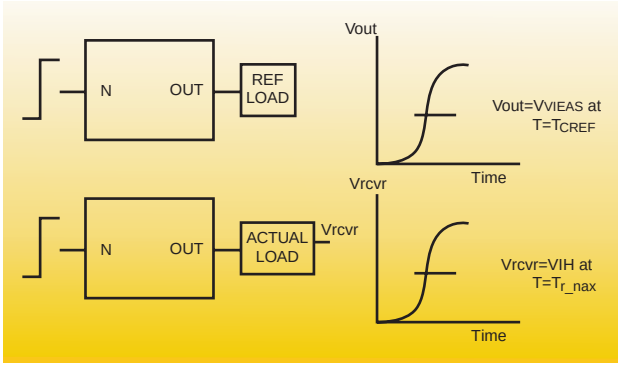

Figure 4 - The timing diagram for TCREF and delay Tr_max.

The compensation time, T_{comp}, and pin-to-pin delay, $T_{pin\text{-}to\text{-}pin}$, are required to correct the predicted delay from the data book value to the actual value. Once T_{comp} and $T_{pin\text{-}to\text{-}pin}$ have been determined, all data book delays to the output pin can be corrected. A separate correction is required if the load is changed, because both T_{comp} and $T_{pin\text{-}to\text{-}pin}$ are load dependent.

Normally, separate timing calculations are required for the rising edge and for the falling edge. This is because the output buffer does not have the same drive current capability when rising as it does when falling. For some buffers, these two times may be comparable, but for others these times may differ by a factor of 2 or more. In particular, open drain (and open collector) drivers have a strong pull down on a bus but very weak pull up, depending on other drivers on their bus to pull the bus up quickly.

Extracting Compensation Time

The compensation time is the time difference between the output voltage crossing VMEAS at the manufacturer's test load and at the actual load. Once calculated, the same T_{comp} applies to all delays from any input pin to this output pin with this load. For other output pins or other loads, the time must be re-measured, because the driver characteristics and load characteristics determine T_{comp}.

The simulated delay T_{CREF} with the manufacturer's test load on the I/O buffer is extracted using a signal integrity simulator (such as HyperLynx) and the buffer's IBIS model. Then the delay T_{vm} under the actual loading (transmission line, receivers, and any terminating components on the signal net) are extracted the same way. The difference $T_{comp}=T_{vm}-T_{CREF}$ is a calibration of the output voltage delay change caused by loading. The value of T_{comp} depends on the simulator; T_{comp} may be positive or negative.

In Figures 5 and 6 the simulation results for a Xilinx Virtex LVCMOS I/O buffer are shown. The LVCMOS output has VMEAS=1.25V and CREF=35pF. For Cload=CREF=35pF, the output delay was 1.2 ns in the HyperLynx simulator. For the actual load of 6" of transmission line and

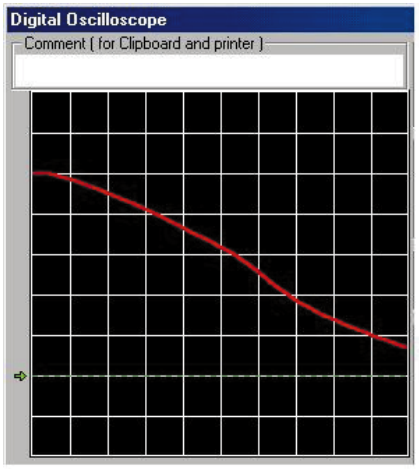

Figure 5 - Simulated delay at C_{load}=CREF. Scope settings are 0.5V/div and 200 ps/div. Vout=VMEAS at T_{CREF}=1.20 ns.

one receiver, the delay was 0.7 ns. We can now calculate the compensation time for the simulator:

$T_{comp} = T_{vm} - T_{CREF} = 0.7 - 1.2 = -0.5$ ns

Extracting the Pin-to-Pin Delay

The pin-to-pin delay, caused by the transmission line and receiver, can be measured directly from a plot of simulation results in a signal integrity simulator. The maximum delay to the receiver is

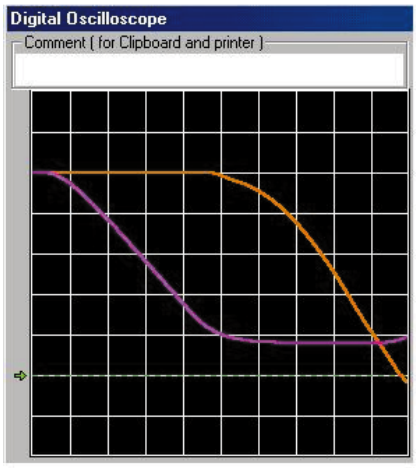

Figure 6 - Simulated delay with 6" transmission line and one receiver. Scope settings are 0.5V/div and 200 ps/div. Vout=VMEAS at T_{vm}=0.7 ns, V_{in}=VIL=0.8V at T_{in}=1.7 ns, and $T_{pin\text{-}to\text{-}pin}$= T_{in}-T_{vm}=1.7-0.7 = 1.0 ns.

when the receiver crosses VIH (rising) or VIL (falling). The delay depends on the signal's interaction with the transmission line, and on the termination strategy. Figure 6 shows the simulated pin-to-pin delay, for the example 6" of transmission line and a 6.5 pF receiver, to be 1.0 ns.

The delay caused by the transmission line is simply the length of the line divided by the speed of the signal in the line: T(line) = Length/vel. The transmission line delay is always positive. Transmission line delays can be anywhere from a few picoseconds to several nanoseconds, depending on the length of the line. For example, the 1" line mentioned previously had a delay of about 200 ps.

The delay of an unterminated receiver is due to the RC impedance at the load, where R is the characteristic impedance of the transmission line and C is the capacitance of the receiver. The time for the receiver to respond is the time required for this RC response to transition from VMEAS to VIH (rising) or to VIL (falling). The receiver delay can be positive or negative, depending on the values of VMEAS and VIH or VIL.

The receiver delay is further influenced by the termination strategy. A series resistor at the driver will reduce the voltage drive available on the transmission line and therefore the drive available to change the voltage on the receiver's internal capacitance, while a parallel (R or RC) termination at the receiver reduces the signal current available to change the voltage on the receiver's internal capacitance. Termination choices can cause significant variation in delay; -50% to +400% variation can be observed in some designs.

The pin-to-pin delay due to the transmission line and receiver (and any associated termination components) is difficult to calculate, particularly when the transmission line branches and connects multiple receivers. Simulation software is normally used for this purpose. Fortunately, the time between the driver's voltage crossing VMEAS and the receiver's state change (maximum delay) can be measured quickly and easily, even for the most complex routing topologies, using the HyperLynx simulator.

Calculating the Total Delay

Once a signal integrity simulator has been used to measure the time delay between the driver pin and the input pin of the receiver, the goal of finding the actual delay can be realized.

The simulator delay includes the buffer delay, the delay down the transmission line, the effects of the receiver capacitance and all termination components, and the voltage change from measuring VMEAS at the driver to VIH or VIL at the receiver. On the other hand, the data book delay includes the buffer delay and the delay

through the IC's logic stages as well as the output buffer driver delay, but only at the manufacturer's test load. By referring back to the diagram in Figure 4, we can now calculate the total delay to the receiver.

The total delay can be calculated, including flight time and simulator calibration effects, as:

$T_{correction} = T_{pin\text{-}to\text{-}pin} + T_{comp}$

$T_{r\_max} = T_{databook} + T_{pin\text{-}to\text{-}pin} + T_{comp} = T_{databook} + T_{correction}$

For our example, with the 6" of transmission line, the Virtex LVCMOS I/O, and using the values from Figures 5 and 6, the correction factor becomes:

$T_{correction} = 1.0 + (-0.5) + = +0.5$ ns.

So, if the data book delay from pin A1 to pin Y9 is Tdatabook=3.5 ns (including logic), then the maximum delay to the receiver is:

T_{r_max} (A1 to Y9) $= T_{databook} + T_{correction} = 3.5 + 0.5$ nsec $= 4.0$ ns

Similarly, if there is a data book delay of 2.7 ns from another input, say A7, to the same output, Y9, then the maximum delay for that path would be:

T_{r_max} (A7 to Y9) $= T_{databook} + T_{correction} = 2.7 + 0.5$ ns $= 3.2$ ns

The maximum delay can be shorter or longer than the data book delay. This corrected delay information can be used to check whether design timing constraints, such as setup and hold times, are satisfied.

Note that it took only two simulations to arrive at the total delay. The first simulation was used to obtain the delay for the manufacturer's test load. The second simulation used the actual net, with its receiver IC and driver IC IBIS models, and the actual net routing and termination components. Finally, the compensation time and the pin-to-pin delay from those simulations are used to correct the total time delay from the input of the first IC to the input of the second IC.

Conclusion

With today's very high speed designs you must consider the transmission line effects of the interconnections between components. By using the HyperLynx signal integrity simulation software, you can precisely determine the overall timing of your design and be assured that your design will work flawlessly under all specified conditions.

For more information on the HyperLynx software, see: www.hyperlynx.com

Dr. Lynne Green has over twenty years of design experience. She recently joined HyperLynx, a division of PADS Software, Inc, as the Product Marketing Engineer for High Speed Products. Previously, at Duet Technologies, Dr. Green designed I/O library cells, and was president of Green Streak Programs, where she did consulting in modeling and simulation. She earned MSEE and PhD degrees in Electrical Engineering at the University of Washington.