FD-based Shift Register V1.0.3

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Features

- Drop-in module for Virtex, Virtex™-E, and Spartan™-II FPGAs
- User definable direction control and bi-directional capability
- Serial and/or parallel inputs and outputs
- Optional clock enable and asynchronous and synchronous controls
- Incorporates Xilinx Smart-IP technology for maximum performance
- To be used with version 2.1i or later of the Xilinx CORE Generator System

Functional Description

The FD-based Shift Register module provides uni-directional or bi-directional shift capability with parallel and/or serial inputs and outputs. Options are also provided for **Clock Enable**, **Asynchronous Set**, **Clear**, and **Init**, and **Synchronous Set**, **Clear** and **Init**. The module can optionally be generated as a Relationally Placed Macro (RPM) or as unplaced logic.

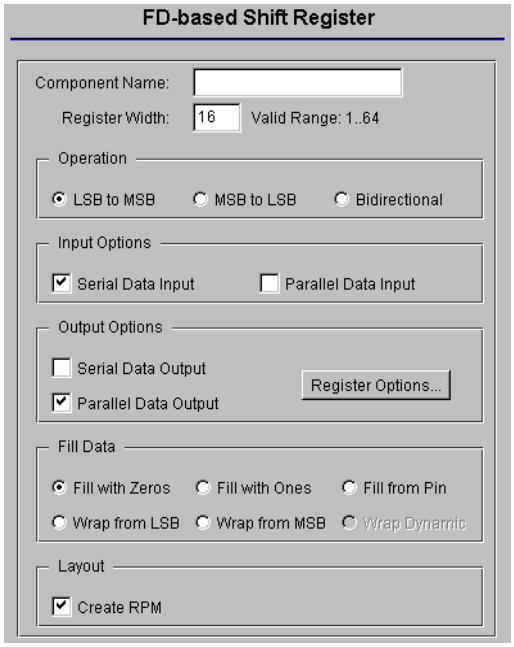

Figure 1: Main FD-based Shift Register Parameterization Screen

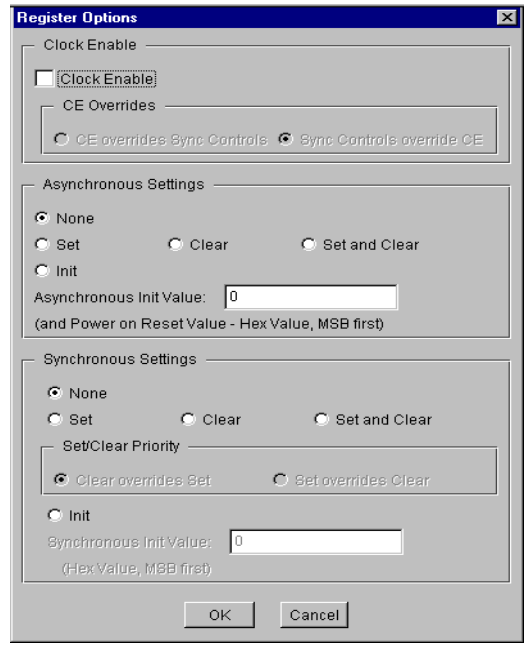

Figure 2: FD-based Shift Register Options Parameterization Screen

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
SDIN	Input	Serial Data Input
D[N:0]	Input	Parallel Data Input
P_LOAD	Input	Parallel Load Input: Controls the loading of the value on D[N:0] into the register. The load is performed synchronously on the next active clock edge where P_LOAD is High.
LSB_2_MSB	Input	Direction control on bi-directional shift registers (High = LSB to MSB, Low = MSB to LSB)
CE	Input	Clock Enable
CLK	Input	Clock: rising edge clock signal
ASET	Input	Asynchronous Set: forces registered output to a High state when driven
ACLR	Input	Asynchronous Clear: forces outputs to a Low state when driven
SSET	Input	Synchronous Set: forces registered output to a High state on next concurrent clock edge
SCLR	Input	Synchronous Clear: forces registered output to a Low state on next concurrent clock edge
AINIT	Input	Asynchronous Initialize: forces registered outputs to user defined state when driven
SINIT	Input	Synchronous Initialize: forces registered outputs to user defined state on next concurrent clock edge
SDOUT	Output	Serial Data Output
Q[N:0]	Output	Parallel Data Output

Note:
All control inputs are Active High. Should an Active Low input be required for a particular control pin an inverter must be placed in the path to the pin. The inverter will be absorbed appropriately during mapping.

Pinout

Signal names for the schematic symbol are shown in Figure 3 and described in Table 1.

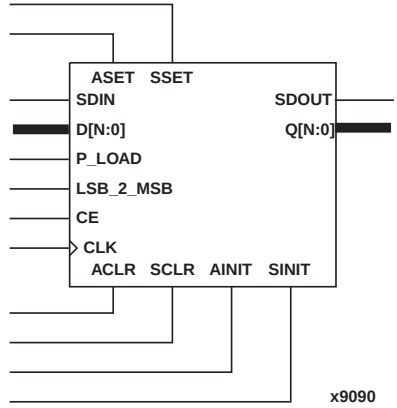

Figure 3: Core Schematic Symbol

CORE Generator Parameters

The main CORE Generator parameterization screen for this module is shown in Figure 1. The parameters are as follows:

- **Component Name**: The component name is used as the base name of the output files generated for this module. Names must begin with a letter and must be composed from the following characters: a to z, 0 to 9 and "_".
- **Register Width**: Enter the width of the shift register. The valid range is 1 to 64. The default value is 16.
- **Operation**: Select the appropriate radio button to specify the required shift direction for the module. The default selection is **LSB to MSB**.
  - **LSB to MSB**: Data is shifted from least significant bit to most significant bit. The setting of the **Fill Data** parameter defines the source for the data that is used to fill Q0. The source for SDOUT is the most significant bit of the register.
  - **MSB to LSB**: Data is shifted from most significant bit to least significant bit. The setting of the **Fill Data** parameter defines the source for the data that is used to fill QN. The source for SDOUT is the least significant bit of the register.
  - **Bidirectional**: Data shift direction is controlled by the LSB_2_MSB pin. When the LSB_2_MSB pin is High the data is shifted from least significant bit to most significant bit and the source for data shifted into the least significant bit is defined by the setting of the **Fill Data** parameter. When the LSB_2_MSB pin is Low, the data is shifted from most significant bit to least significant bit and the source for data shifted into the most significant bit is defined by the setting of the **Fill Data** parameter. Irrespective of the

value on the LSB_2_MSB pin, the SDOUT output is always sourced by the MSB of the shift register.

- **Input Options**:
  - **Serial Data Input**: This checkbox defines the presence of the SDIN pin on the module. If this checkbox is not checked, the **Fill Data** option **Fill from Pin** is not available. The default setting is checked.
  - **Parallel Data Input**: This checkbox defines the presence of the D[N:0] bus and the P_LOAD pin on the module. The default setting is checked.

  Note that the module can be generated without serial or parallel inputs. In this case the **Asynchronous Init Value** or **Synchronous Init Value** core defines the shift register pattern.
- **Output Options**: The module must be generated with at least one type of output.
  - **Serial Data Output**: This checkbox defines the presence of the SDOUT pin on the module. The default setting is unchecked.
  - **Parallel Data Output**: This checkbox defines the presence of the Q[N:0] bus on the module. The default setting is checked.
  - **Register Options**: Clicking on this button brings up the Register Options parameterization screen (see Figure 2).
- **Fill Data**: Select the appropriate radio button to define the source for the fill data. The default selection is **Fill with Zeros**.
  - **Fill with Zeros**: The fill data tied to zero.
  - **Fill with Ones**: The fill data tied to one.
  - **Fill from Pin**: The fill data is provided externally via the SDIN pin.
  - **Wrap from LSB**: The fill data is provided from the output of the least significant bit.
  - **Wrap from MSB**: The fill data is provided from the output of the most significant bit.
  - **Wrap Dynamic**: This selection is only available when the **Operation** is set to **Bidirectional**. The source of fill data is controlled by the LSB_2_MSB pin. When the LSB_2_MSB pin is high, the fill data is sourced from the least significant bit of the register. When the LSB_2_MSB pin is low, the fill data is sourced from the most significant bit of the register.
- **Create RPM**: When this box is checked the module is generated with relative location attributes attached. The resulting placement of the module is in a column with two bits per slice. The default operation is to create an RPM.

  Note that when a module is created as an RPM it is possible that one or more of the module dimensions may exceed those of the device being targeted. If this is the case mapping errors will occur and the compilation process will fail. In this case the module can be re-generated with the **Create RPM** checkbox unchecked. This will reduce the performance of the module since the placement will no longer be controlled.

The Register Options parameterization screen for this module is shown in Figure 2. The parameters are as follows:

- **Clock Enable**: When this box is checked the module is generated with a clock enable input. The default setting is unchecked.
- **CE Overrides**: This parameter controls whether or not the SSET, SCLR, and SINIT inputs are qualified by CE. This parameter is only enabled when a **Clock Enable** input has been requested.

  When **CE Overrides Sync Controls** is selected an active level on any of the synchronous control inputs will only be acted upon when the CE pin is also Active. Note that this is not the way that the dedicated inputs on the flip-flop primitives work, and so setting the **CE Overrides** parameter to **CE Overrides Sync Controls** will force any synchronous control functionality to be implemented using logic in the Look Up Tables (LUTs) preceding the output register. This results in increased resource utilization.

  When **Sync Controls Override CE** is selected an active level on any of the synchronous control inputs is acted upon irrespective of the state of the CE pin. This setting allows the dedicated inputs on the flip-flop primitives to be used for the synchronous control functions provided that asynchronous controls are not requested. If both asynchronous and synchronous controls are requested, the synchronous control functionality must be implemented using logic in the LUTs preceding the output register. In this case, the CE input has to be gated with the synchronous control inputs so that each synchronous control input and the CE input can generate a CE signal to the flip-flops. This results in a performance degradation for the module due to the additional gating in the CE path.

  The default setting is **Sync Controls Override CE** so that the more efficient implementation can be generated.
- **Asynchronous Settings**: All asynchronous controls are implemented using the dedicated inputs on the flip-flop primitives. The module can be generated with the following asynchronous control inputs by clicking on the appropriate button:
  - **None**: No asynchronous control inputs. This is the default setting.
  - **Set**: An ASET control pin is generated.
  - **Clear**: An ACLR control pin is generated.
  - **Set and Clear**: Both ASET and ACLR control pins are generated. ACLR has priority over ASET when both are asserted at the same time.
  - **Init**: An AINIT control pin is generated which, when asserted, will asynchronously set the output register to the value defined in the **Asynchronous Init Value** text box.

- **Asynchronous Init Value**: This text box accepts a hex value whose equivalent bit width must be less than or equal to the **Register Width**. If a value is entered that has fewer bits than the **Register Width** it is padded with zeros. An invalid value is highlighted in red in the text box.
  The value specified in this text box also functions as the power on reset value for the output register. The default value is 0.
- **Synchronous Settings**: When no asynchronous controls are requested (i.e. the **Asynchronous Setting** is **None**) the synchronous controls can be implemented using the dedicated inputs on the flip-flop primitives. There are exceptions to this which are described in the sections for the **Set/Clear Priority** and **CE Overrides** parameters.
  When asynchronous controls are present any synchronous control functionality must be implemented using logic in the Look Up Tables (LUTs) preceding the output register. With modules where a non-registered output is not required there are combinations of parameters that allow this logic to be absorbed into the same LUTs used to implement the function. In cases where this absorption is not possible the synchronous control logic will require an additional LUT per output bit.
  The module can be generated with the following synchronous control inputs by clicking on the appropriate button:
  - **None**: No synchronous control inputs. This is the default setting.
  - **Set**: An SSET control pin is generated.
  - **Clear**: An SCLR control pin is generated.
  - **Set and Clear**: Both SSET and SCLR control pins are generated. SCLR/SSET priority is defined by the setting of the **Set/Clear Priority** parameter.
  - **Init**: An SINIT control pin is generated which, when asserted, will synchronously set the output register to the value defined in the **Synchronous Init Value** text box.
- **Set/Clear Priority**: By selecting the appropriate radio button the relative priority of SCLR and SSET can be controlled. This parameter is only enabled when **Set and Clear** is selected for **Synchronous Settings**.

  A setting of **Clear Overrides Set** corresponds to the native operation of the flip-flop primitive. This setting will result in a more efficient implementation when asynchronous controls are not requested. A setting of **Set Overrides Clear** can only be implemented using logic in the LUTs preceding the output register.

  The default setting is **Clear Overrides Set** so that the dedicated inputs on the flip-flops can be used if available.
- **Synchronous Init Value**: This text box accepts a hex value whose equivalent bit width must be less than or equal to the **Register Width**. If a value is entered that has fewer bits than the **Register Width** it is padded with zeros. An invalid value is highlighted in red in the text box. This parameter is only enabled when the **Synchronous Settings** parameter is set to **Init**. The default value is 0.

Parameter Values in the XCO File

Names of XCO file parameters and their parameter values are identical to the names and values shown in the GUI, except that underscore characters (_) are used instead of spaces. The text in an XCO file is case insensitive.

Table 3 shows the XCO file parameters and values, and summarizes the GUI defaults. The following is an example of the CSET parameters in an XCO file:

```
CSET component_name = abc123
CSET register_width = 16
CSET operation = lsb_to_msb
CSET serial_data_input = TRUE
CSET parallel_data_input = FALSE
CSET serial_data_output = FALSE
CSET parallel_data_output = TRUE
CSET fill_data = fill_with_zeros
CSET create_rpm = TRUE
CSET clock_enable = FALSE
CSET ce_overrides = sync_controls_override_ce
CSET asynchronous_settings = none
CSET async_init_value = 0000
CSET synchronous_settings = none
CSET sync_init_value = 0000
CSET set_clear_priority = clear_overrides_set
```

Core Resource Utilization

These modules require 1 flip-flop per shift register bit.

Modules with parallel load, bi-directional capability and/or synchronous controls that cannot be implemented using the dedicated flip-flop control inputs require a LUT per shift register bit.

When the bidirectional mode is selected and the **Fill Data** parameter is **Fill from Pin** or **Wrap Dynamic** a single additional LUT is required per module.

When the synchronous control functionality cannot be implemented using the dedicated control inputs of the flip-flop (i.e. when asynchronous controls are also requested) and the **CE Overrides** are set to **Sync Controls Override CE** an additional LUT per module is required.

Table 2: XCO File Values and Default Values

Parameter	XCO File Values	Default GUI Setting
component_name	ASCII text starting with a letter and based upon the following character set: a..z, 0..9 and _	blank
register_width	Integer in the range 1 to 64	16
operation	One of the following keywords: lsb_to_msb, msb_to_lsb, bidirectional	lsb_to_msb
serial_data_input	One of the following keywords: true, false	true
parallel_data_input	One of the following keywords: true, false	false
serial_data_output	One of the following keywords: true, false	false
parallel_data_output	One of the following keywords: true, false	true
fill_data	One of the following keywords: fill_with_zeros, fill_with_ones, fill_from_pin, wrap_from_msb, wrap_from_lsb, wrap_dynamic	fill_with_zeros
create_rpm	One of the following keywords: true, false	true
clock_enable	One of the following keywords: true, false	false
ce_overrides	One of the following keywords: sync_controls_override_ce, ce_overrides_sync_controls	sync_controls_override_ce
asynchronous_settings	One of the following keywords: none, set, clear, set_and_clear, init	none
async_init_value	Hex value whose value does not exceed $2^{number\_of\_outputs} - 1$	0
synchronous_settings	One of the following keywords: none, set, clear, set_and_clear, init	none
sync_init_value	Hex value whose value does not exceed $2^{number\_of\_outputs} - 1$	0
set_clear_priority	One of the following keywords: clear_overrides_set or set_overrides_clear	clear_overrides_set

Ordering Information

This core is downloadable free of charge from the Xilinx IP Center (www.xilinx.com/ipcenter), for use with version 2.1i and later versions of the Xilinx Core Generator System. The Core Generator System is bundled with the Alliance and Foundation implementation tools.

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