LD-based Parallel Latch V1.0.3

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Features

- Drop-in module for Virtex, Virtex™-E and Spartan™–II FPGAs
- 1 to 64 bits wide
- Optional Gate Enable input
- Optional Asynchronous Set, Clear and Init
- Optional Synchronous Set, Clear and Init
- Incorporates Xilinx Smart-IP technology for maximum performance
- To be used with version 2.1i and later of the Xilinx CORE Generator System

Functional Description

The latch based data register is a member of the Base-BLOX series of building blocks for the Virtex architecture. Options are provided for **Gate Enable**, **Asynchronous Set**, **Clear and Init**., and **Synchronous Set**, **Clear and Init**, and Synchronous vs. Asynchronous priority. The module can optionally be generated as a Relationally Placed Macro (RPM) or as unplaced logic. When an RPM is generated the logic is placed in a column.

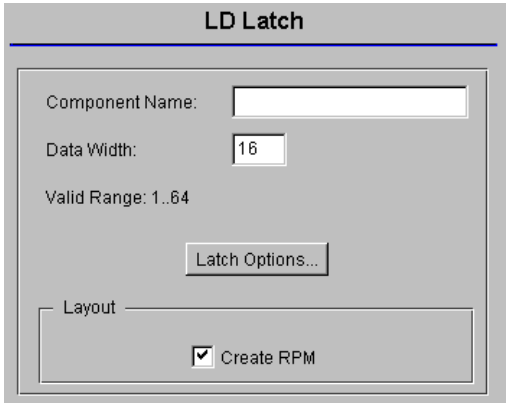

Figure 1: Main LD Register Parameterization Screen

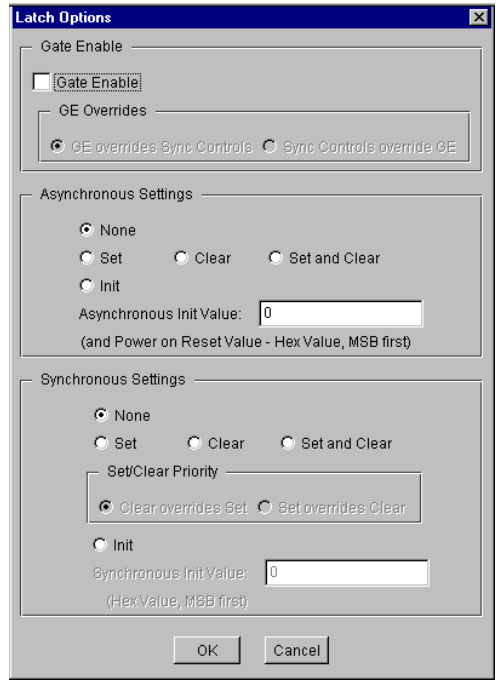

Figure 2: Latch Options Parameterization Screen

Pinout

Signal names are shown in Figure 3 and described in Table 1.

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
D[N:0]	Internal	Internal data input connection to optional output register
GE	Input	Gate Enable
G	Input	Gate: latched when High, transparent when Low
ASET	Input	Asynchronous Set: forces all outputs to a High state when driven
ACLR	Input	Asynchronous Clear: forces all outputs to a Low state when driven
SSET	Input	Synchronous Set: forces all outputs to a High state on next transparent state
SCLR	Input	Synchronous Clear: forces all outputs to a Low state on next transparent state
AINIT	Input	Asynchronous Initialize: forces the outputs to a user defined state when driven
SINIT	Input	Synchronous Initialize: forces the outputs to a user defined state on next transparent state
Q[N:0]	Output	Data output

Note:
All control inputs are Active High. If an Active Low input is required for a particular control pin, an inverter must be placed in the path to the pin. The inverter will be absorbed appropriately during mapping.

CORE Generator Parameters

The main CORE Generator parameterization screen for this module is shown in Figure 1. The parameters are as follows:

- **Component Name**: The component name is used as the base name of the output files generated for this module. Names must begin with a letter and must be composed from the following characters: a to z, 0 to 9 and "_".
- **Data Width**: Enter the latch width from the pull down menu. The valid range is 1 to 64. The default value is 16.
- **Latch Options**: Clicking on this button brings up the Latch Options parameterization screen (see Figure 2).
- **Create RPM**: When this box is checked a module will be generated with relative location attributes attached. The resulting placement of the module will be in a column with two bits per slice. The default setting is to create an RPM.

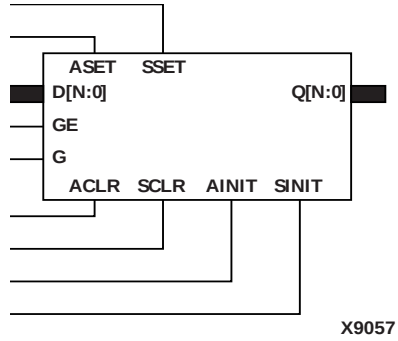

Figure 3: Core Schematic Symbol

The Latch Options parameterization screen for this module is shown in Figure 2. The parameters are as follows:

- **Gate Enable**: When this box is checked the module is generated with a gate enable input. The default setting is unchecked.
- **GE Overrides**: This parameter controls whether or not the SSET, SCLR, and SINIT inputs are qualified by GE. This parameter is only enabled when a **Gate Enable** input has been requested.

  When **GE Overrides Sync Controls** is selected an active level on any of the synchronous control inputs will only be acted upon when the GE pin is also Active.

  When **Sync Controls Override GE** is selected an Active level on any of the synchronous control inputs is acted upon irrespective of the state of the GE pin. This setting allows the dedicated inputs on the flip-flop primitives to be used for the synchronous control functions provided that asynchronous controls are not requested. If both asynchronous and synchronous controls are requested, the synchronous control functionality must be implemented using logic in the LUTs preceding the output register. In this case, the GE input has to be gated with the synchronous control inputs so that each synchronous control input and the GE input can generate a GE signal to the flip-flops. This results in a performance degradation for the module due to the additional gating in the GE path.

  The default setting is **Sync Controls Override GE** so that the more efficient implementation can be generated.
- **Asynchronous Settings**: All asynchronous controls are implemented using the dedicated inputs on the latch primitives. The module can be generated with the

following asynchronous control inputs by clicking on the appropriate button:
  - **None**: No asynchronous control inputs. This is the default setting.
  - **Set**: An ASET input pin is generated.
  - **Clear**: An ACLR input pin is generated.
  - **Set and Clear**: Both an ASET and an ACLR input pins are generated. ACLR has priority over ASET when both are asserted at the same time.
  - **Init**: An AINIT input pin is generated which, when asserted, will asynchronously set the latch to the value defined in the Asynchronous Init Value text box.
- **Asynchronous Init Value**: This text box accepts a hex value whose equivalent bit width must be less than or equal to the **Data Width**. If a value is entered that has fewer bits than the **Data Width** it is padded with zeros. An invalid value is highlighted in red in the text box. The value specified in this text box also functions as the power on reset value for the output register. The default value is 0.
- **Synchronous Settings**: Synchronous controls for latches can only be implemented using logic in the Look Up Table (LUT) preceding the latch.
  The module can be generated with the following synchronous control inputs by clicking on the appropriate button:
  - **None**: No synchronous control inputs. This is the default setting.
  - **Set**: An SSET control pin is generated.
  - **Clear**: An SCLR control pin is generated.
  - **Set and Clear**: Both SSET and SCLR control pins are generated. SCLR/SSET priority is defined by the setting of the **Set/Clear Priority** parameter.
  - **Init**: An SINIT control pin is generated which, when asserted, will synchronously set the output register to the value defined in the **Synchronous Init Value** text box.
- **Set/Clear Priority**: By selecting the appropriate radio button the relative priority of SCLR and SSET can be controlled. This parameter is only enabled when **Set and Clear** is selected for **Synchronous Settings**.

  The default setting is **Clear Overrides Set**.
- **Synchronous Init Value**: This text box accepts a hex value whose equivalent bit width must be less than or equal to the **Data Width**. If a value is entered that has fewer bits than the **Data Width** it is padded with zeros. An invalid value is highlighted in red in the text box. This parameter is only enabled when the **Synchronous Settings** parameter is set to **Init**. The default value is 0.

Parameter Values in the XCO File

The names of XCO file parameters and parameter values are identical to the names and values shown in the GUI, except that underscore characters (_) are used instead of spaces. The text in an XCO file is not case sensitive.

Table 2 shows the XCO file parameters and values, as well as summarizing the GUI defaults. The following is an example of the CSET parameters in an XCO file:

```
CSET component_name = abc123
CSET data_width = 16
CSET create_rpm = TRUE
CSET clock_enable = FALSE
CSET ge_overrides = sync_controls_override_ge
CSET asynchronous_settings = none
CSET async_init_value = 0000
CSET synchronous_settings = none
CSET sync_init_value = 0000
CSET set_clear_priority = clear_overrides_set
```

Core Resource Utilization

This core uses one latch primitive per bit. For cases where any synchronous control functionality is required there is an extra cost of one LUT per bit. In the case where **Sync Controls Override GE** an additional LUT is required per module.

Ordering Information

This core is downloadable free of charge from the Xilinx IP Center (www.xilinx.com/ipcenter), for use with the Xilinx Core Generator System version 2.1i and later. The Core Generator System 2.1i tool is bundled with the Alliance 2.1i and Foundation 2.1i implementation tools.

To order Xilinx software contact your local Xilinx sales representative at www.xilinx.com/company/sales.htm.

Table 2: XCO File Values and Default Values

Parameter	XCO File Values	Default GUI Setting
component_name	ASCII text starting with a letter and based upon the following character set: a.. z, 0..9 and _	blank
data_width	Integer in the range 2 to 64	16
create_rpm	One of the following keywords: true, false	true
clock_enable	One of the following keywords: true, false	false
ge_overrides	One of the following keywords: sync_controls_override_ge, ge_overrides_sync_controls	sync_controls_override_ge
asynchronous_settings	One of the following keywords: none, set, clear, set_and_clear, init	none
async_init_value	Hex value whose value does not exceed $2^{data\_width} - 1$	0
synchronous_settings	One of the following keywords: none, set, clear, set_and_clear, init	none
sync_init_value	Hex value whose value does not exceed $2^{data\_width} - 1$	0
set_clear_priority	One of the following keywords: clear_overrides_set or set_overrides_clear	clear_overrides_set