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Features

- Supports 4000X, 9500, Spartan, Spartan™-II, Virtex™, and Virtex™-E devicesCompact UART
- 8-bit characters
- TxC / RxC (16 times the desired output baud rate)
- 1 start bit / 1 stop bit
- Polling and interrupt modes
- Flexibility for adding other features

Applications

The C_UART core is used in serial data communications applications.

AllianceCORE™ Facts	
Core Specifics	
See Table 1	
Provided with Core	
Documentation	Core Design Document
Design File Formats	EDIF netlist, .ngo, Verilog Source RTL available extra
Constraints File	C_UART.ucf
Verification	VHDL testbench, test vectors
Instantiation Templates	VHDL, Verilog
Reference Designs & Application Notes	None
Additional Items	None
Simulation Tool Used	
1076 compliant, VHDL simulator, Verilog simulator	
Support	
Support provided by CAST, Inc.	

Table 1: Core Implementation Data

Supported Family	Device Tested	Macrocells[2]	Product Terms[2]	I/O[1]	Performance[2] (MHz)	Special Features	Xilinx Tools
9500	9572-7	68	163	26	100[3]	None	M1.5
9500XL	9572XL-5	68	161	26	178.5[3]	None	M1.5

Supported Family	Device Tested	CLBs[5]	Clock IOBs	IOBs[1]	Performance (MHz)	Special Features	Xilinx Tools
4000XL	4013XL-08	43	2	24	94	None	M1.5i
Spartan	S30-4	46	2	24	65	None	M1.5i
Virtex	V50-6	42[4]	2	24	142	None	M1.5i

Notes:
1. Assuming all core I/O are routed off-chip.
2. CPLD figures stated are optimized for density.
3. Max CPLD performance measured for CLK16 input.
4. Utilization numbers for Virtex are in CLB slices.
5. Optimized for speed.

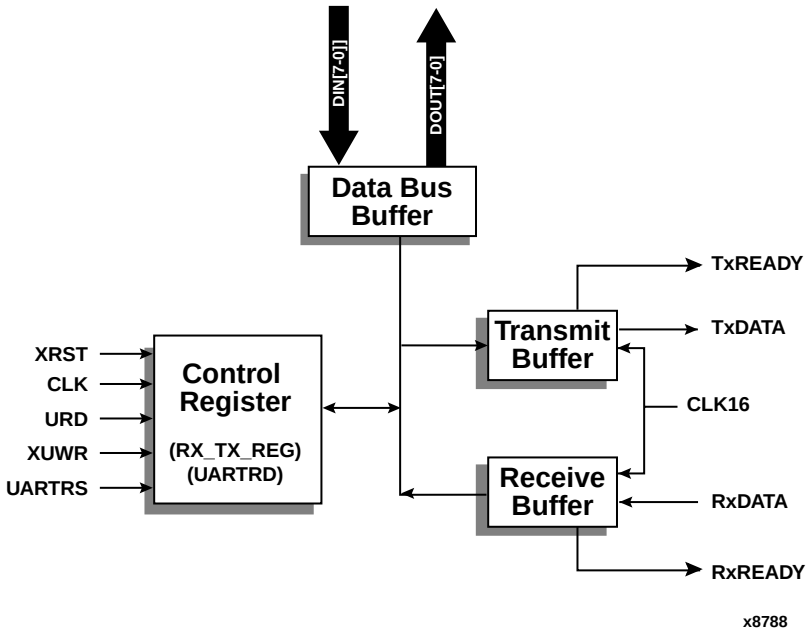

Figure 1: C_UART Compact UART Block Diagram

General Description

The C_UART core is a generic universal asynchronous receiver/transmitter (UART) and can be used to implement a peripheral data communication device. The designer can program the core with an 8-bit CPU.

Functional Description

The C_UART core is partitioned into modules as shown in Figure 1 and described below.

Control Register

RX_TX_REG - UART R/W Data Register

7	6	5	4	3	2	1	0
d	d	d	d	d	d	d	d

The Data Register is used for reading data from the receiver or writing data to the transmitter. This register is cleared during reset.

UARTRD - UART Read STATUS Register

7	6	5	4	3	2	1	0
0	0	0	0	0	0	n	n

Bit 0 RxREADY	n=0	Rx BUFFER FULL
	n=1	Rx BUFFER EMPTY
Bit 1 TxREADY	n=0	Tx BUFFER EMPTY
	n=1	Tx BUFFER FULL

The Status Register maintains information about the current operational status of the UART. During reset, bit 0 of the register is set, and bit 1 is cleared.

Data Bus Buffer

The Data Bus Buffer is used to interface with the external Data Bus. Its contents are either written to the RX_TX_REG or are loaded from it depending on the state of the Control Register.

Transmit Buffer

The Transmit Buffer is used to hold the data being transmitted out of the C_UART. It is loaded from the Data Bus Buffer. The data is output serially to the TxDATA pin by the data clock (CLK16).

Receive Buffer

The Receive Buffer is used to hold data as it comes into the C_UART via the RxDATA pin input serially by the data clock (CLK16).

Core Modifications

The C_UART core can be customized to include:

- Different Character length
- Parity
- Different Start/Stop bits
- Modem Functions

Please contact CAST directly for any required modifications.

Pinout

The pinout of the C_UART core has not been fixed to specific FPGA I/O, allowing flexibility with a users application. Signal names are shown in the block diagram in Figure 1, and in Table 2.

Verification Methods

The C_UART core's functionality has been extensively tested with a VHDL testbench and a large number of test patterns.

Recommended Design Experience

The user must be familiar with HDL design methodology as well as instantiation of Xilinx netlists in a hierarchical design environment.

Ordering Information

The C_UART core is available from CAST, Inc. Please contact CAST, Inc. directly for pricing and information.

The C_UART core is licensed from Moxsyn S.R.L.

Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
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Table 2: Core Signal Pinout

Signal	Signal Direction	Description
XRST	Input	Master Reset
CLK	Input	System Clock
URD	Input	Decoded UART Read
XUWR	Input	Decoded UART Write Control for Transmitter Register
UARTRS	Input	Register Select 0 = Status Register 1 = R/W Data Register
DIN[7:0]	Input	Input Data Bus
DOUT[7:0]	Output	Output Data Bus
TxREADY	Output	Transmitter Empty (ready to accept new character)
TxDATA	Output	Transmitter Data
CLK16	Input	Transmit/Receive Master Clock
RxDATA	Input	Receiver Data
RxREADY	Output	Receiver Ready (character ready to be transferred to CPU)

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