UTOPIA_L2_TX UTOPIA Level 2 PHY Side TX Interface

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CSELT S.p.A

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Features

- Supports Spartan™-II, Virtex™, and Virtex™-E devices
- Protocol conversion from UTOPIA level 2, TX mode, PHY side to Pb
- Customizable VHDL source code available allowing generation of different netlist versions
- DPRAM-based internal buffering for clock decoupling
- Customized testbench for pre- and post-synthesis verification supplied with the module
- Core customization
  - Interface data width (8/16 bits)
  - Cell error detection mode (data parity, short cell, long cell)
  - Cell error management mode (no action, flag, discard)
  - Physical idle cell generation (yes/no)
  - Reset mode (synchronous /asynchronous)
  - Size of the internal buffer memory

Applications

- Physical Layer ATM circuits

AllianceCORE™ Facts

Core Specifics[1]		
Supported Family	Spartan	Virtex
Device Tested	S20-3	V50-6
CLBs[2]	239	76
Clock IOBs	2	2
IOBs[3]	41	41
Performance (MHz)	38	61
Xilinx Tools	M1.5i/M2.1i	M1.5i/M2.1i
Special Features	TBUFs, SelectRAM	BlockRAM
Provided with Core		
Documentation		User Manual
Design File Formats		EDIF netlist, XNF netlist, VHDL source available extra
Constraints File		Top_U2PTX_nl.ncf
Verification		VHDL testbench
Instantiation Templates		VHDL, Verilog
Reference Designs & Application Notes		None
Additional Items		None
Simulation Tool Used		
Synopsys VSS		
Support		
Design and customization support provided by CSELT		

Notes:
1. Data refer to the following customization:
   8-bit interface;
   Data parity, short and long cell error flags;
   Physical idle cell generation;
   Asynchronous reset; and
   Internal buffer size = 4 ATM cells
2. Utilization numbers for Virtex are in CLB slices
3. Assuming all core I/Os (excluding N_CTSENB) are routed off-chip

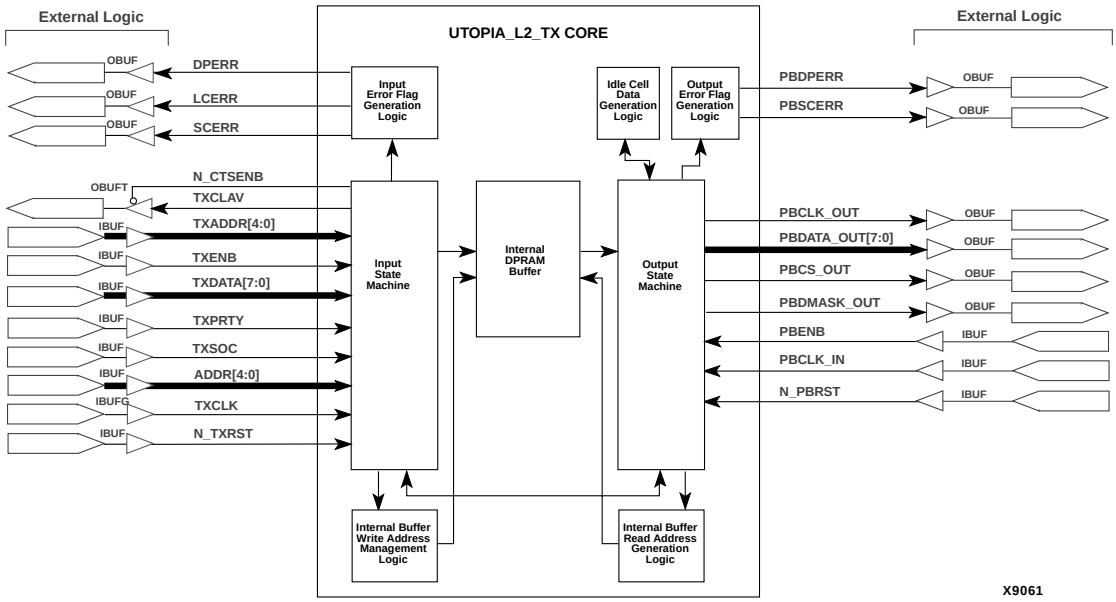

Figure 1: UTOPIA_L2_TX Block Diagram

General Description

The UTOPIA_L2_TX Level 2 Interface core implements an interface between two ATM cell transfer protocols: the ATM Forum UTOPIA level 2 protocol (PHY TX side, cell level) and the Pb protocol (as defined in RACE BLNT). Either the 8-bit or the 16-bit data transmission mode can be implemented, depending on the selected customization.

The core can store a limited amount of ATM cells in a local buffer for clock decoupling purposes. Besides, it can handle cell length errors and/or parity errors in the cell data in accordance with a customizable error handling mode; one out of three different handling modes (no action, flag, discard) can be implemented.

The Absolute Maximum ratings, Operating Conditions, DC Electrical Specifications and Capacitances depend on the Xilinx device selected for implementation and can be retrieved in the corresponding Xilinx datasheet.

Functional Description

The internal architecture of the UTOPIA_L2_TX core is shown in Figure 1. A brief description of the operation of each module follows.

Input State Machine

The Input State Machine handles the UTOPIA level 2 PHY TX interface and the write port of the DPRAM cell buffer. Besides, it performs cell integrity controls and flags or discards faulty cells in accordance with the error handling policy set for the core implementation.

It has to be pointed out that only short cells and cells with data parity errors can be discarded, while long cells cannot. The above happens because a received cell becomes available to the output interface as soon as the last valid cell byte/word is received. So, the first extra byte/word of a long cell could be received when the corresponding cell is already being output – or, even, has already been completely output. For the same reason, long cell error flags are not forwarded to the Output Error Flag Generation Logic.

Output State Machine

The Output State Machine handles the Pb output interface and the read port of the DPRAM cell buffer. It also controls the timing of the output interface error flags and the output of idle cells when no data are available in the internal DPRAM buffer (if the above options have been selected for implementation).

If the short cell discard option is not implemented, short cells are completed with unpredictable data. Long cells are always truncated.

Internal Buffer Write/Read Address Management Logic

The Address Management modules handle the generation of the read and write addresses of the DPRAM cell buffer. The cell buffer is structured as a paged memory; the mem-

ory page size is one ATM cell (53 bytes in 8 bit mode, 54 bytes in 16 bit mode). The Address Management modules exchange information about the page being read/written, that is used by the Input and Output State Machines to detect the buffer full and empty status.

Since Write and Read Address Management logic are clocked by different clocks, dual-rank synchronizers are used to decouple the connections between them. Also, the page address counters are implemented as Gray counters to avoid race conditions.

Input Error Flag Generation Logic

The Input Error Flag Generation Logic handles the output of the error flags generated by the input interface. Input error flags are raised as soon as the error condition causing them occurs, and last for one input clock cycle.

Output Error Flag Generation Logic

The Output Error Flag Generation Logic stores the error flags generated by the input interface. Output error flags are raised when the first byte/word of the corresponding cell is output, and last till the end of the cell. Only short cell errors and data parity errors are stored (see the Input State Machine description for details).

Internal DPRAM Buffer

The internal DPRAM buffer is a dual port RAM in which cell data are stored. The buffer memory implementation depends on both the device family (DPRAM primitive size is 16 bits for Spartan SelectRAM and 4 Kbits for Virtex Block-RAM) and on the value of the NPAGES generic parameter set for the desired implementation.

Idle Cell Data Generation Logic

The Idle Cell Data Generation logic is a state machine that generates on command the data corresponding to an idle cell for the ATM physical layer, as specified in the ITU-T I-432 recommendation. Physical layer idle cells are used to ensure stream continuity in cell based data transmission, and must be removed by the receiver end of the physical link.

Pinout

The pinout of this core has not been fixed to a specific FPGA I/O allowing flexibility with a user's application. Signal names are shown in the block diagram in Figure 1 and described in Table 1.

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
UTOPIA Interface		
TXCLAV	Output	Cell available flag; three-state
TXADDR[4:0]	Input	Address bus
TXENB	Input	Transmission enable
TXDATA[7:0]	Input	Data; 8/16 bits port size based on DMODE generic
TXPRTY	Input	Data parity
TXSOC	Input	Start of cell flag
TXCLK	Input	Data clock
Pb Interface		
PBCLK_OUT	Output	Data clock
PBDATA_OUT[7:0]	Output	Data; 8/16 bits port size based on DMODE generic
PBCS_OUT	Output	Start of cell flag
PBDMASK_OUT	Output	Data mask
Control and Status Ports		
DPERR	Output	Data parity error flag (UTOPIA interface)
LCERR	Output	Long cell error flag (UTOPIA interface)
SCERR	Output	Short cell error flag (UTOPIA interface)
N_CTSENB	Output	TXCLAV output enable, Active Low
ADDR[4:0]	Input	UTOPIA port address
PBDPERR	Output	Data parity error flag (Pb interface)
PBSCERR	Output	Short cell error flag (Pb interface)
PBENB	Input	Pb interface output enable
Clock and Reset Ports		
N_TXRST	Input	Reset (TXCLK clock)
PBCLK_IN	Input	Pb data clock input
N_PBRST	Input	Reset (PBCLK_IN clock)

Table 2: Core Parameters (VHDL Generics)

Parameter	Description
DMODE	Data transfer mode (8/16 bit)
ERRCHECK	Data error check configuration
IDLEGEN	Idle cell generation mode(active/inactive)
NPAGES	Internal buffer depth (cells)
RSTMODE	Reset mode (synchronous/asynchronous)

Core Modifications

CSELT provides netlist customized to the user's requirements. The UTOPIA_L2_TX core source code is parametric. Parameters shown in Table 2 are implemented as a set of generics in the synthesizable VHDL source code of the core. These parameters allow the user to specify some architectural and functional features, so as to adapt the netlist to a specific design or application.

Verification Methods

Extensive functional (pre-synthesis) and timing (post-synthesis) simulation has been performed for different values of the core parameters, using the Synopsys VSS simulator. Simulation scenarios (including data and command files) and parametric test bench used for design verification are provided with the core.

The parametric test bench is composed of a programmable ATM cell generator with UTOPIA level 2 interface, ATM side. The generated cell stream is customized; cell generation commands are read from a text file. Cell stream customizing includes header data, (random or user-defined), payload data (random, counter, fixed or user-defined), period and size of transmission holes, error injection (data errors, cell length errors).

Recommended Design Experience

Experience with the Xilinx design flow and ATM transmission system design is recommended to the users of the netlist version of the core. For the source code version, users should also be familiar with the Synopsys FPGA synthesis tools (VHDL Compiler, FPGA Compiler) and simulator (VSS).

Ordering Information

The UTOPIA_L2_TX core is provided under license by CSELT S.p.A for use in Xilinx programmable logic devices. Please contact CSELT S.p.A for information about pricing, terms and conditions of sale.

Related Information

A copy of the interface specification is available at the ATM Forum web site:

ftp.atmforum.com/pub/approved-specs/af-phy-0039.000.pdf

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
URL: www.xilinx.com

For general Xilinx literature, contact:

Phone: +1 800-231-3386 (inside the US)
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E-mail: literature@xilinx.com

For AllianceCORE™ specific information, contact:

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E-mail: alliancecore@xilinx.com
URL: www.xilinx.com/products/logicore/alliance/tblpart.htm

UTOPIA_L2_TX
Implementation Request Form

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CSELT configures and ships Xilinx netlist versions of the UTOPIA_L2_TX core customized to your specification. Please fill out and fax this form so that CSELT can respond with an appropriate quotation that includes performance and density metrics for the target Xilinx FPGA.

From: _____

Company:_____

Address:_____

City,State,Zip:_____

Country:_____

Phone:_____

FAX:_____

E-mail:_____

Implementation Issues

1. Data transfer mode (8 bit / 16 bit): _____

2. Flag cells with data parity errors? _____

3. Discard cells with data parity errors? _____

4. Flag short cells?_____

5. Discard short cells? _____

6. Flag long cells?

7. Discard long cells (when possible)?

8. Internal buffer depth (cells):

9. Idle cell generation required?

10. Reset mode (sync/async):

Business Issues

1. Indicate timescales of requirement:
_____ date for decision
_____ date for placing order
_____ date of delivery

2. Indicate your area of responsibility:
_____ decision maker
_____ budget holder
_____ recommender

3. Has a budget been allocated for the purchase?
Yes _____ No _____

4. What volume do you expect to ship of the product that will use this core? _____

5. What major factors will influence your decision?
_____ cost
_____ customization
_____ testing
_____ implementation size

6. Are you considering any other solutions? _____