XF-RSENC Reed Solomon Encoder

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Features

- Supports 4000X, Spartan, Spartan™-II, Virtex™, and Virtex™-E devices
- Core design is customized using the following specifications:
  - Primitive polynomial
  - Generator polynomial
  - Number of parity symbols

AllianceCORE™ Facts

Core Specifics	
See Table 1	
Provided with Core	
Documentation	Core Documentation
Design File Formats	VHDL/Verilog RTL files
Constraints File	.ucf
Verification	testbench, Test vectors
Instantiation Templates	VHDL, Verilog
Reference designs & application notes	Sample Implementation in Verilog or VHDL
Additional Items	Warranty by MDS
Simulation Tool Used	
Model Technology, Silos	
Support	
Support provided by Memec Design Services.	

Table 1: Example Implementations

	XF-RSENC-DVB Example #1	XF-RSENC-DVB Example #2	XF-RSENC-DVB Example #3	XF-RSENC-INTELSAT Example #4
Parity Symbols	16	16	16	14,16,18,20
Bits/Symbol	m=8	m=8	m=8	m=8
Supported Family	Spartan	4000XL	Virtex	Virtex
Device Tested	S05-3	4005XL-09	V50-6	V150-4
CLBs: Core +Ext Logic	76[2]	101[3]	94[3,4]	138[2,4]
IOBs: Core[1]	19	19	19	24
IOBs: Core +Ext Logic	19	19	19	24
Clock IOBs	1	1	1	1
Max Data Rate	368 MBit	624 MBit	904 MBit	10 MBit
Performance	46 MHz	78 MHz	113 MHz	44 MHz
Xilinx Tools	M1.5i	M1.5i	M1.5i	M1.5i
Special Features	None	None	None	SelectRAM

Notes:
1. Assume all core signals are routed off-chip.
2. Optimized for area during synthesis.
3. Optimized for speed during synthesis.
4. Virtex utilization numbers are in CLB slices.

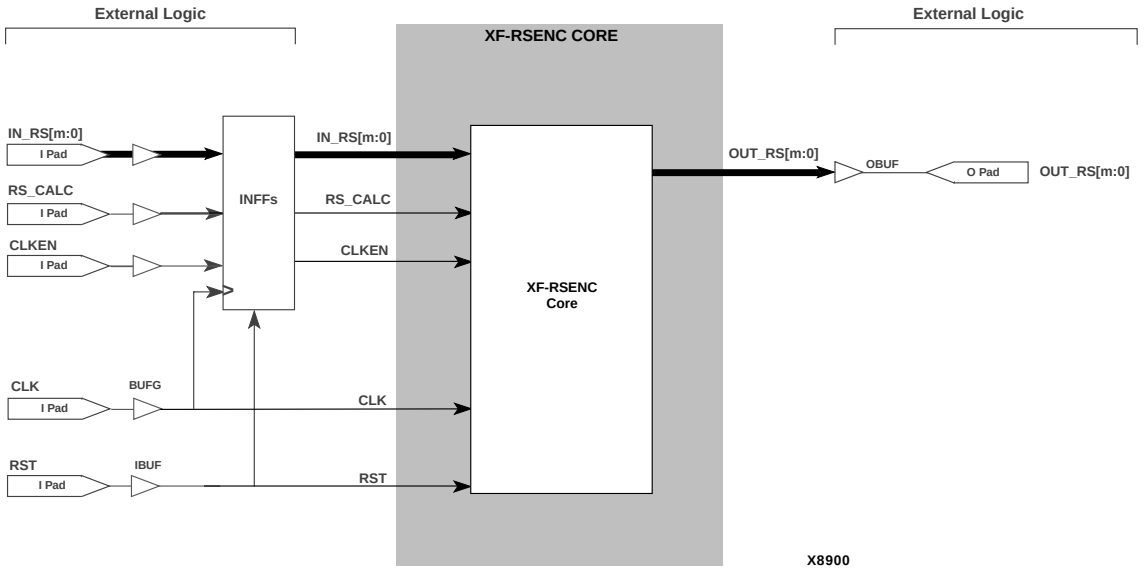

Figure 1: XF-RSENC Core with External Logic (Examples 1, 2, 3)

PostScript error (undefined, get)

Figure 2: Reed Solomon Encoder Functional Block Diagram (Examples 1, 2, 3)

  - Symbol size
  - Symbol clock rate
  - System clock rate
- Message Block length configured by end user
- Continuous or burst mode operation
- Supports high speed applications (>900Mbps)
- Simple core interface for ease of integration
- Includes Verilog or VHDL source code

Applications

- Data communication channels
- DTV/HDTV broadcast
- Data storage systems
- Satellite communications

General Description

Reed-Solomon coding is a method of forward error correction in the form of block coding. Block coding consists of calculating a number of parity symbols over a number of