The Evans & Sutherland Ensemble Image Generator

Virtex and Spartan FPGAs help Evans & Sutherland accelerate their development schedule, and roll in new features during and after the main design cycle.

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Since the early 1970s, E&S has produced industry-leading computer image generators for commercial and military pilot training. These special-purpose graphics computers generate realistic and detailed out-the-window and sensor simulations in real-time for training people to operate a wide range of vehicles including aircraft, ships, trains, tanks, and automobiles.

Ensemble System Requirements

In April 1998, a small engineering team began working on the product definition of the company's first PC-based image generator for the simulation market, using graphics accelerator boards based on the company's latest generation of REALimage technology. Other image generators made by the company use custom ASICs designed specifically for the demanding task of real-time image generation.

While based on a standard graphics chip, these new PCI form-factor graphics boards have been specifically tailored for the simulation market and contain simulation-specific features not generally available on standard PC-based graphics accelerator boards. This new image generator system, Ensemble™, is software compatible with the company's current high-end image generator, Harmony™.

The engineering team defined three graphics accelerator boards, Quartet™, Duet™, and Solo™, with different levels of performance to meet different price points. All of the cards have the following features designed specifically for the simulation market:

- Order-independent antialiasing with four subsamples per pixel generated with no impact to pixel fill rate.
- Video genlock for synchronizing the video rates of multiple cards.
- Edge blending to roll off the video intensity along the edges to allow seamless overlaps of channels when using projectors.
- Own-ship lighting to simulate the effect of vehicle lights illuminating the scene implemented in hardware so as not to impact the rendering performance.
- Postprocessing effects to simulate infrared or night vision goggle sensor channels.
- A double-buffered overlay plane used for displaying the symbols typically seen on a heads-up display.

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Quartet Board Block Diagram

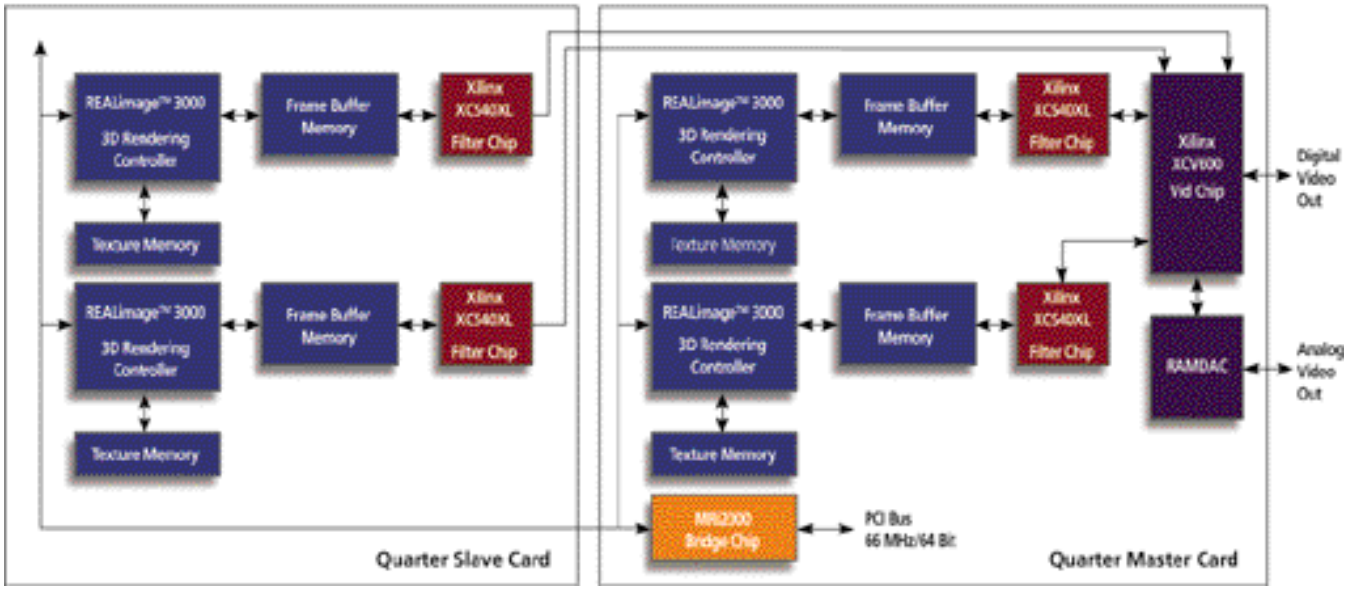

Figure 1

Selecting a Technology

Most of these simulation-specific features are implemented in a postprocessing device, called the Vid chip, which fits between the frame buffer and the RAMDAC, and is the key element in differentiating the Ensemble graphics accelerators from boards developed for the more traditional PC workstation, gaming, or home markets.

Due to its central role in the operation of the boards, the engineering team focused on selection of the technology for the Vid chip early in the design process. The engineering team wanted to use an FPGA for the Vid chip, but were not sure that FPGAs would be dense enough to fit all of the feature set, or fast enough to meet the requirements of postprocessing video "on-the-fly."

Standard REALimage-based graphics accelerator boards have a gate array called the Pixel Converter 2000 that fits in the same place that the Vid chip occupies on the Ensemble boards. The Vid chip implements most of what is in the Pixel Converter 2000 and adds to that all the simulation-specific post-processing features.

Evaluating the Alternatives

The engineering team took the Verilog code for the Pixel Converter 2000 ASIC and, without modification, compiled the code using the Xilinx and Altera synthesis tool chains. The initial Xilinx target was a member of the XC4000 family.

The results showed that the Pixel Converter code, which is implemented in a 50K gate device, almost filled up the largest Xilinx and Altera parts available at the time, and ran only at half the required frequency. Note that this was without modifying the code in any way to make it map more efficiently to the FPGA architecture, but the results left the team uneasy about the prospects of implementing the Vid chip in a FPGA.

At this time, Xilinx provided E&S with preliminary information about their new Virtex family. As soon as Xilinx delivered an early release of the tool chain with Virtex support, we recompiled the Pixel Converter code and targeted for Virtex. This time the results showed that the Pixel Converter code occupied about 50% of an XCV300 and ran at about 75% of the required speed. These results led us to

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believe that, with some work, the Vid chip could be implemented in a Virtex part and meet the system timing requirements. The team targeted the Vid chip to run at 80 MHz, which would support a 1280x1024-resolution screen refreshed at 85 Hz.

Implementing the Design

The Quartet board (Fig. 1), which is actually a two-board set with four REALimage 3000 chips, has the highest pixel fill performance of any PC-based graphics accelerator card currently produced by E&S. It can process 400 million textured, shaded, and antialiased pixels per second.

The Quartet boards are designed to use the Virtex XCV600 for the Vid and four Spartan XCS40XL "Filter" chips. The Filter chips implement the antialiasing filter and reduce the pin count to the Vid chip.

Detailed design of the Quartet board and the Vid chip began in August of 1998. The first prototype Quartet boards were powered on for the first time in early November 1998. A prototype Ensemble system was demonstrated three weeks later at a trade show for the simulation industry.

Using Virtex FPGAs to implement the Vid chip allowed the Ensemble engineering team to pursue this aggressive design schedule. The team was able to commit to pin-outs of the Vid and Filter chips early, to begin the circuit board layout while continuing to roll features into the design of the FPGAs. The availability of large amounts of block SelectRAM in the Virtex device also allowed us to implement many of our sophisticated post-processing algorithms.

Conclusion

Without the density and speed of the Virtex parts, the Vid chip probably would have been implemented in a gate array, causing a much longer development cycle for the Ensemble boards. The engineering team would have had less opportunity to roll in new and enhanced features during and after the main design cycle. Σ

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