The Virtex Family– a Powerful ASIC Alternative

With the success of the Virtex FPGA family, programmable logic technology has reached density, feature, and performance levels that make it a viable ASIC alternative in system-level applications.

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The ASIC industry is moving toward deep sub-micron processes and standard cell methods instead of gate array design implementations. However, standard cell technology, though it's great for enabling system-level designs, is complex in both architecture and implementation. Standard cell design cycles are becoming more complex, with rigorous verification and testing required in the pre-silicon phase.

Non Recurring Engineering charges (NRE) and minimum volume requirement hurdles are becoming more and more prohibitive, and leading standard cell vendors must choose both customers and applications carefully, because of the high up-front investment required by customer and vendor. However if you simply want to get to market quickly, with designs that work and fit within your budget, Virtex FPGAs may offer the right solution for you.

Design Cycles Stretch Out

Throughout the early 1990's, ASIC software developers focussed on creating algorithms and point tools that reduced die size. Process technology suddenly jumped from 1.0-µ geometries to the deep-submicron 0.13-µ processes in development today. ASIC tools lost their foothold and are just now strengthening their ability to comprehend the issues of interconnect, power, and simultaneously switching outputs (SSO) that are so critical in deep-submicron design. ASIC Designers spend less and less time in the "window of innovation" (authoring, creating, and determining optimal feature sets) and too much time in the simulation and verification stages of the design cycle. In fact, studies show that only 20% of the typical ASIC design process is spent in the innovation stage.

Figure 1 shows the relative time spent in each of the design tasks required in today's ASIC environment. More point tools are required, and the time spent in verification becomes the overriding task. Test development must also be factored in. Studies have shown that up to 40% of the entire design process can be spent in test development.

Typical ASIC Design Process
(Source: Electronic Systems, Jan. 99)

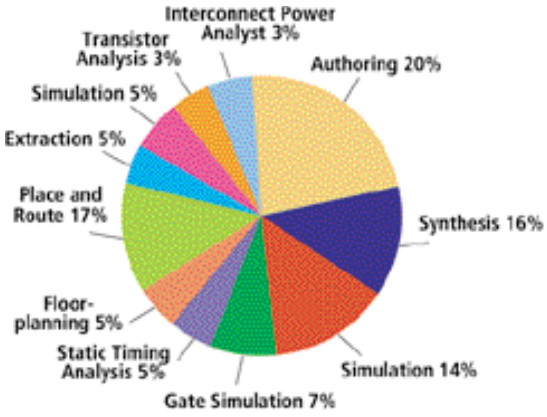

Figure 1

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In the ASIC environment, exhaustive simulation and verification is crucial, because designers can't afford mistakes. NRE charges that cover the costs of prototyping were actually decreasing throughout the 1980's and early 1990's, as third party EDA companies picked up more of the design tasks. But NRE charges for deep-submicron devices radically reverse that trend. Mask sets for one 0.18µ device can run well over $200,000. With average standard cell design cycles running 9 to 12 months, a single mistake found during test, after the prototype cycle is complete, can put a project six months behind schedule and require a second NRE.

Virtex FPGAs Solve Deep-Submicron ASIC Design Dilemmas

Because our devices are programmable, we have "pre-engineered" many of the issues that plague system-level ASIC designers today. Each Virtex device is already specified, verified, and tuned for proper I/O performance. SSO, power, and interconnect issues have been resolved prior to the production release of the FPGA family.

In the development phase, you are working with actual silicon, so modeling, simulation, and verification results reflect actual silicon performance. Thus, you can spend more time in the "window of innovation," working on authoring, feature development, and system-level integration, without sweating through a silicon prototyping phase before any real in-system testing can begin.

Figure 2 shows the relative design-cycle times for ASICs vs. FPGAs. With decreases in process technology, design cycles have actually increased. FPGAs still have the shortest design cycles, and Integrated Circuit Engineering estimates that development costs are 92% less for and FPGA than for a comparable ASIC solution.

Design Tools Further the FPGA Advantage

Time to market is one of the most crucial issues you face. Shortening the design cycle is critical. As an ASIC alternative, FPGA design tools play a major role in increasing the advantage through dramatic reductions in compile times and a streamlined design flow.

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In the past, FPGA designers were accustomed to compile times on the order of 10,000 gates/hour. Through new algorithms, Xilinx place and routing tools compile at the rate of 100,000 gates/minute. This provides the ability to achieve multiple design turns per day, which allows more time to spend in the window of innovation, creating an optimal design. The advantage of quickly realizing a design change in actual, qualified silicon can not be accomplished in an ASIC design flow.

The ASIC design flow is powerful but complex, and requires lots of tools which are usually very expensive. Ultimately you are not in full control of the tools. The FPGA design flow requires fewer steps, which gives you the flexibility to control the entire design methodology.

A significant time saving example is the built-in FPGA scan insertion. Scan is used to test "stuck-at" faults within the silicon, and FPGAs are 100% tested. However, for ASICs,

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Relative Design-Cycle Times

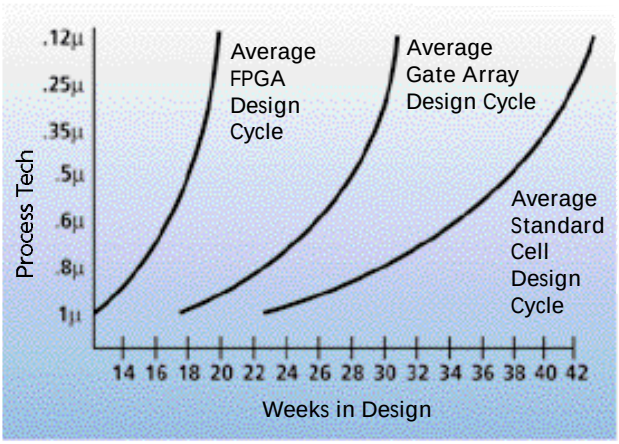

Figure 2

there is a lengthy verification process to ensure minimum coverage. The FPGA design tools are designed to place, route, and download the bitstream, allowing in-system verification. In the event of an Engineering Change Order (ECO), you can implement the change, perform functional verification, and place and route the design on real silicon.

The place and route tool outputs a standard delay format (SDF) file for use with static timing analyzers to aid in reaching timing convergence. Thus, an ECO can be implemented within the original design, instead of having to fix a board, or add components.

The ASIC Bar is Raised

Not only have system-level ASIC design cycles stretched out and NREs increased, but minimum order quantities have been raised as well. Eight- to twelve-inch wafers can yield hundreds of 0.18µ die. Wafer fabrication economics dictate that steady, high volume brings down costs, stabilizes manufacturing lines, and best utilizes expensive resources.

Many pure-play foundries require minimum purchases of 20,000 to 50,000 ASIC devices as a starting point for engagement. Because the investment is high for the ASIC vendor and for the customer, many first tier ASIC vendors have very exclusive customer criteria and accept only the highest volume, and most-stable projects from well-established customers. If your projects do not fit 1st tier ASIC vendor criteria, having the Virtex FPGA path for system-level design is a crucial alternative.

Summary

Our feature-rich Virtex devices, with up to one million system gates, including Block RAM, DLL's, and pre-verified core solutions, could not have been introduced at a more appropriate moment in the system-level design revolution.

As complex ASIC design becomes more expensive and tougher to complete in today's time-critical markets, Virtex FPGAs create real, programmable alternatives without the prohibitive development costs and drawbacks of an ASIC solution. Σ

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