Xilinx DSP

High Performance
Signal Processing

January 1998

XILINX®

New High Performance DSP Alternative

New advantages in FPGA technology and tools:

Xilinx DSP offers a new alternative to ASICs, fixed function DSP devices, and DSP processors. This DSP solution is achieved through the introduction of larger FPGAs, efficient DSP algorithms, and tools to automate the design process.

Performance equivalent to an ASIC:

Just like custom silicon, Xilinx FPGAs implement the same high performance parallel processing but FPGAs are standard, off-the-shelf programmable (and re-programmable) devices. High level DSP building blocks (cores) are easily accessible with point-and-click design tools. Semiconductor processing technology has driven down the cost of FPGAs and HardWire equivalents making them cost effective compared with the difficult to implement custom chip alternative.

More flexible than fixed function DSP devices:

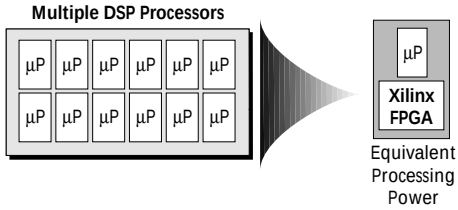
Fixed function, standard product DSP devices can also fall prey to this new technology. Xilinx FPGAs offer the flexibility to implement exactly what is required for a given application through highly parameterized building blocks. FPGAs are usually one or two process generations ahead of these standard function devices giving FPGAs a cost advantage.

Higher performance and lower cost than DSP processors:

Relative to DSP processors, Xilinx FPGAs offer the same flexibility plus an incredible performance advantage at a fraction of the cost. FPGAs can act as co-processors to implement the calculation intensive, high sample rate portions of the signal processing. This reduces the burden on the DSP processor allowing it to implement the code intensive portions of the algorithm and utilize the existing libraries of DSP processor legacy code.

Xilinx DSP Comparison With Processors

The performance of standard DSP processors is adequate for many applications. However, once you reach the performance limit of the fastest DSP processor the traditional way to achieve higher performance has been to add more processors. The performance gain that comes with each additional processor is small when compared to the increase in cost, board space, power consumption, and development time. In addition, multiple processors require complex real-time multi-processor code that is difficult to develop and debug. The millions of MACs (multiply accumulates) per second that is possible to achieve with multiple processors comes at a high cost.



Many applications demand low cost and performance that is beyond the capabilities of standard processors. Today's solution is to add Xilinx DSP, not more processors. With Xilinx you can do billions of MACs in a single programmable part through parallel processing. Xilinx FPGAs are standard, off-the-shelf parts that are configured to implement DSP functions parameterized to your specific needs. Now the flexibility of a processor can be extended using a hardware solution with parallel processing capabilities.

The Xilinx DSP solution offers all of the traditional advantages of programmable logic, such as instant prototyping and fast time to market. But in addition, Xilinx offers the highest performance and the lowest cost through a unique combination of architectural features, software tools, and automatic ASIC migration.

Examples of Xilinx DSP Designs

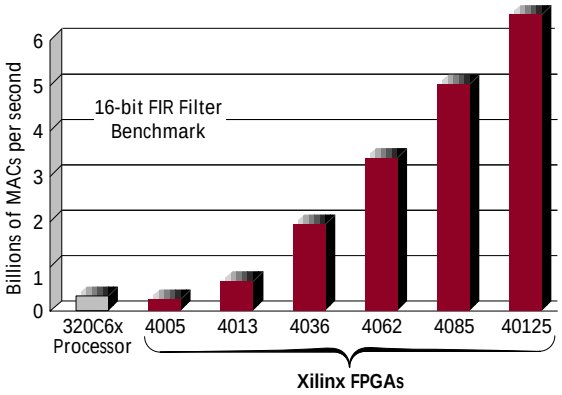
Digital cellular communications	Telephony line testers
Cell phone testers	Digital subscriber loops
Wireless local loop	Cable modems
Wireless communications	Set top boxes
PCS base stations	Copiers
Modem banks, (T1 modem banks)	Multi-function radios
Imaging	HDTV

Xilinx DSP is used today in a variety of applications in many market areas.

One Xilinx FPGA Has the Performance of Ten DSP Processors

Compare the number of multiply accumulates (MACs) possible using the Xilinx DSP solution to that of the fastest DSP processor. The smallest device in the Xilinx XC4000XL family offers comparable performance.

The performance of Xilinx DSP scales with the number of logic cells (device size) because as more logic cells are added, more parallel processing is possible. The XC4085XL device offers at least ten times the performance of any DSP processor.

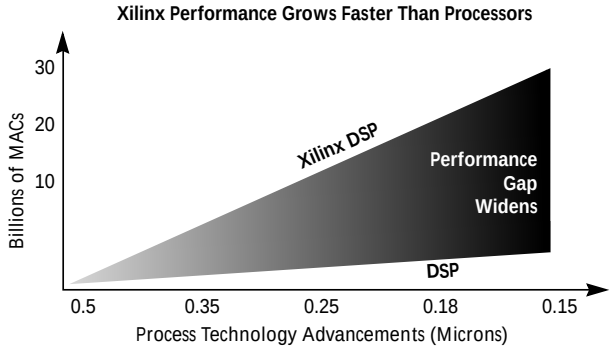


Xilinx FPGAs extend the performance of DSP processors.

The performance of Xilinx FPGAs will rapidly grow over time as our standard product FPGAs migrate to smaller process geometries. The performance gain for FPGAs is a result of two factors: higher clock rates and an increase in the number of logic cells. Higher clock rates can be achieved with smaller geometries. And, higher clock speed allows cores designed for the previous devices to run faster without the need for redesign. Even more significant is the fact that process shrinks permit a large increase in the number of logic cells that will fit on a single FPGA device. This factor overshadows the relatively modest increase in clock rate because the additional logic cells can be used to increase performance through more parallelism that comes from reducing device geometries. Xilinx DSP automatically benefits from both of these factors.

DSP processors can also take advantage of the higher clock rates, however, processors require new architectures with multiple CPUs, multiple MAC units, and so on, to benefit from the increase in the number of transistors that come from process shrinks. And, it becomes a progressively more difficult task to design new silicon implementations with multiple processors. In addition, the complexity of the real time software required to implement actual applications becomes a limiting factor for the user.

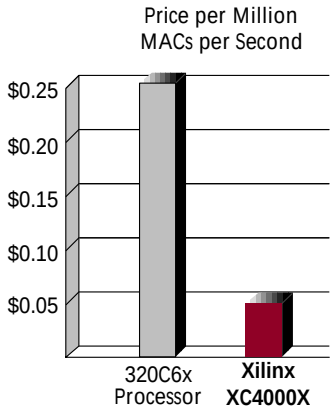
The end result is that the performance capabilities of the Xilinx DSP solution will continue to grow faster than the performance of standard processor solutions, and the Xilinx solution will be less complicated to implement.



Low Cost

The processor industry has established a cost benchmark based on the number of multiply-accumulates per second that a solution can provide. Processors are just now breaking the 30 cent per million MACs per second barrier. Today, the Xilinx XC4000XL programmable solution is under five cents per million MACs per second, a more than 80% cost savings. By migrating to Xilinx HardWire™ FpgASIC, cost can be further reduced to almost a penny per million MACs per second.

The XC4000 family is the industry's most successful Field Programmable Gate Array family. Because of its tremendous momentum, it is quickly moving down the process technology curve, further reducing the cost of the Xilinx programmable solution.



HardWire™ Conversion

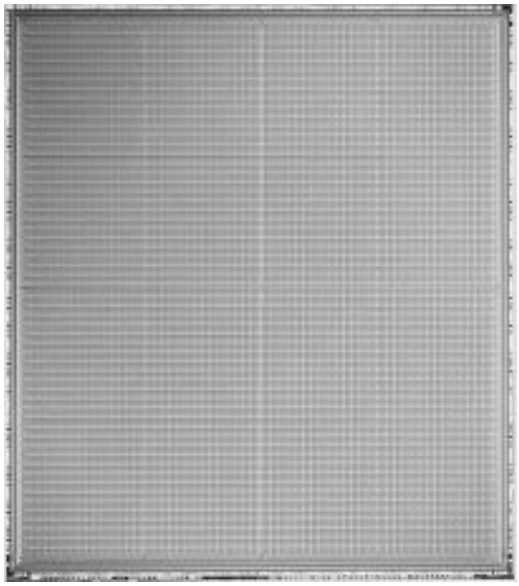
No Engineering Required

For high volume production, FPGAs can be automatically converted to an ASIC equivalent through the Xilinx patented HardWire conversion process. All of the conversion is done by Xilinx, and no new test vectors are required. You can move on to the next project instead of spending valuable time on cost reduction. This is the fastest way to the lowest cost production solution. HardWire devices can reduce the cost of a programmable solution by as much as 90%.

Using Xilinx FPGAs, you can design single-chip DSP system-level solutions that automatically can be converted to HardWire ASIC devices. This design approach opens up access to the cost and high performance of custom silicon in ways that are not possible with any other solution.

Distributed Arithmetic Requires Distributed RAM

A Xilinx XC4000 FPGA is a large matrix of Configurable Logic Blocks (CLBs), each of which has two 16-word by 1-bit RAM primitives. The XC40125XL contains over 9,000 RAMs along with flip-flops and programmable interconnect lines. Each CLB can be used to implement logic, ROMs (look-up tables), single or dual port RAMs. The memory (called SelectRAM™) is distributed throughout the chip, not combined in fixed size blocks.

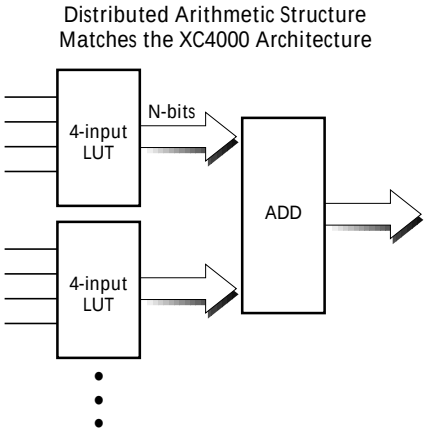


Die Photo illustrates the regular, scalable structure of the distributed memory architecture of Xilinx FPGAs

A key element of the Xilinx DSP solution includes the use of a unique approach known as Distributed Arithmetic (DA). DA algorithms are a perfect match for a distributed RAM architecture.

Using this matched algorithm/architecture combination, complex functions fit into FPGAs with efficiency that rivals custom chips. ASIC gate counts for equivalent functions are much higher than in non-DSP applications, reflecting the efficiency of the Xilinx FPGA architecture for DSP applications.

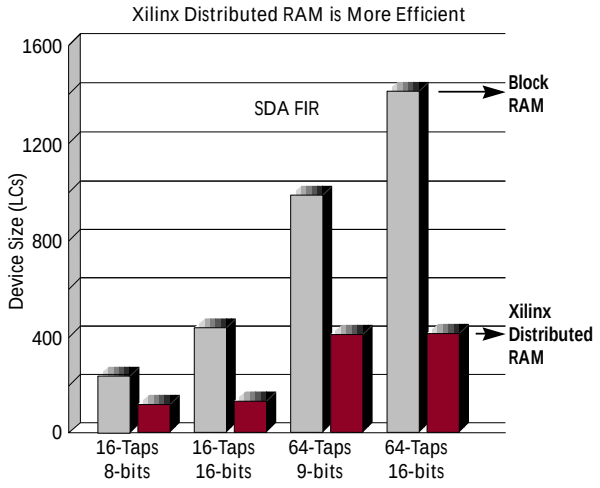
Look-up tables (LUTs) and adders are combined to solve a wide variety of problems. Much of the arithmetic complexity is implemented in look-up tables. For example, in serial distributed arithmetic (SDA) FIR filters, the look-up tables contain pre-calculated sums of filter coefficients. By using the incoming sample data as address inputs to the table, many operations are performed in parallel. The FIR filter is built without any multipliers, dramatically reducing the number of resources needed to implement the function.



DSP functions can be broken down into LUT / accumulate implementations that are a perfect fit with the Xilinx FPGA architecture.

More Efficient FIR Filters and Adaptive Filters

Distributed RAM is also useful for buffering sample data streams in a FIR filter. For a 16-bit data word, 16 flip-flops are required for each data sample. To build 500 taps would require over 8,000 flip-flops, more than most FPGAs currently contain. But with distributed RAM, large shift registers with many intermediate taps can be built from RAM primitives. As a result, hundreds of taps operating at sample rates exceeding 100 million samples per second will fit in a single Xilinx device.

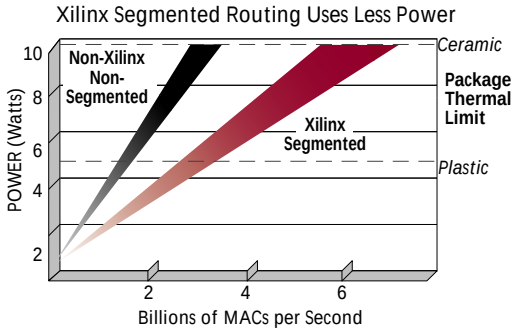


Distributed RAM makes possible the implementation of a time-skew buffer in RAM instead of flip-flops, resulting in a 50% reduction in filter size.

Adaptive filters can also benefit from distributed RAM. The ROM based LUTs in SDA (serial distributed arithmetic) or PDA (parallel distributed arithmetic) FIR filter cores can be replaced with RAM based LUTs which allows coefficients to be updated instantly. Implementations of large adaptive filters are not possible in FPGAs without distributed RAM.

Segmented Routing = Lower Power Dissipation

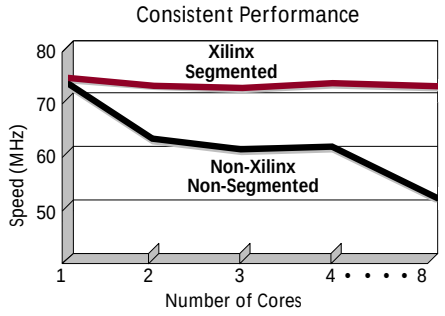
An additional feature of the unique architecture of the Xilinx DSP solution is lower power consumption compared to non-segmented routing architectures. This is especially important in DSP applications where power is often the limiting factor. Billions of MACs require many nodes to switch at high frequencies and this increases the AC power consumption for CMOS IC process technology. The key to reducing the power dissipation for a given process geometry is to shorten the length of the metal lines that are used to interconnect the programmable logic blocks. Xilinx segmented routing uses shorter metal lines, which reduce capacitance and thus reduce power by at least a factor of two. You get more MACs before reaching the package thermal limit.



Segmented Routing + LogiCOREs = Predictability

The Xilinx segmented routing architecture has advantages beyond power savings. It permits the size and performance of a core to be specified before the design has been implemented. Performance is consistent as cores are added to a large device and performance is the same for any size device in the XC4000X family. Only the combination of Xilinx segmented routing architecture and LogiCORE™ methodology make this possible.

Cores implemented in FPGAs without segmented routing suffer from unpredictable performance degradation as you add additional cores to the device. In addition, the long metal lines in non-segmented FPGAs must get even longer as the device size becomes larger and this results in a 30% reduction in performance between the smallest and the largest device.



DSP LogiCORE modules use only local routing resources. This 12-bit multiplier core benchmark illustrates the performance and predictability of Xilinx DSP over competing FPGAs.

Complex Design Made Easy

CORE Generator

Most of the DSP design work has already been done for you with the Xilinx CORE Generator and DSP LogiCORE products. This new tool delivers system level DSP functional blocks automatically. Pre-verified, performance characterized cores are selected from a hierarchical library and then parameterized to your exact specifications. Just connect the blocks to create a design that will process millions of samples per second without the need to develop real-time processor code.

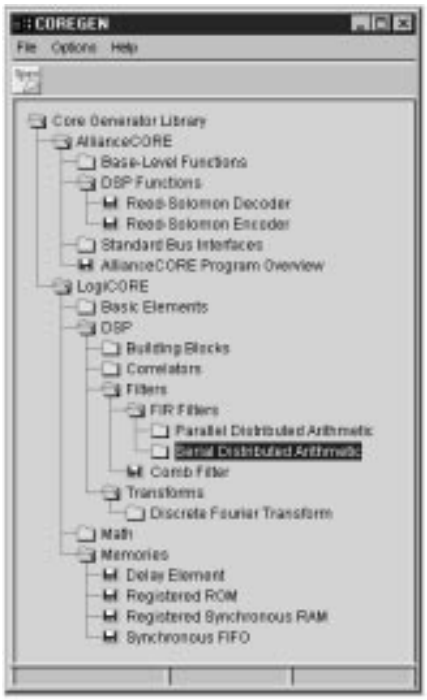
The CORE Generator generates the cores to your specification and then delivers them for use with most standard hardware design environments such as VHDL, Verilog or schematic capture. The CORE generator outputs a logic netlist and a behavioral model along with a symbol for use with schematic capture, or instantiation code for VHDL or Verilog.

If schematic capture is used for the top-level design, the interconnected, parameterized cores resemble your system-level block diagram. If you use a high level language approach, use VHDL or Verilog code to connect the parameterized cores and integrate them into your overall design. The CORE Generator delivers HDL instantiation code 'snippets' for each LogiCORE that can be pasted into the overall HDL file to complete the design. You can use the behavioral models to test the functionality.

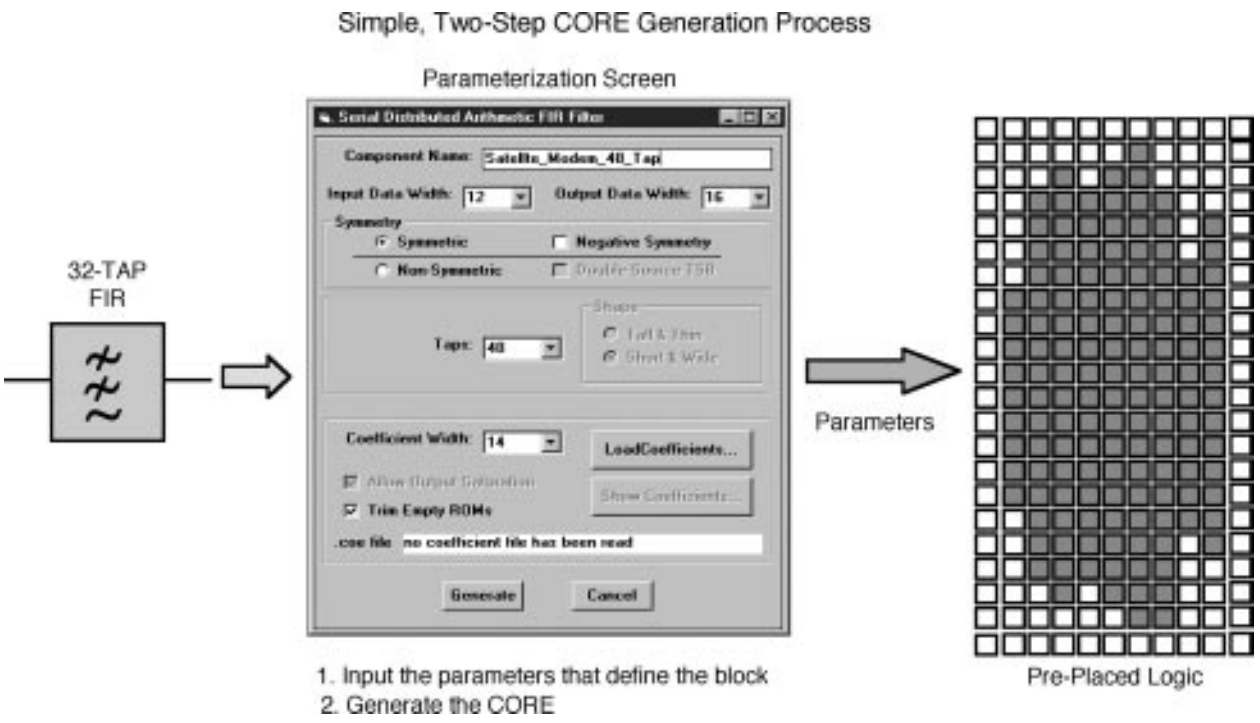
The CORE Generator is the only high level FPGA design tool that produces the logic for each parameterized core in parallel with a physical layout. This logic plus layout allows you to know the size and performance of each system core before the design is implemented. The DSP Core Generator produces the best possible FPGA design, matching the performance of hand-tuned implementations. The performance for each core is specified in the LogiCORE data sheet.

Compatible With VHDL, Verilog, and Schematic Top Level Design

Designers access DSP cores through an intuitive hierarchical 'tree' format with the modules sorted into functional categories. When a particular type of function is selected, a parameterization dialog box opens for that core. User-selected parameters are then passed to the appropriate module generator for implementation. On-line error checking ensures that only valid parameters are specified. Help and data sheets are available on-line.



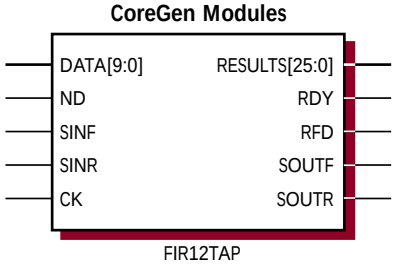
Both the user interface and its underlying structural framework are designed to be flexible, allowing automatic addition of new cores through a 'plug & play' feature. Xilinx LogiCORE products along with third-party AllianceCOREs products can be added to the CORE Generator by simply downloading files and placing them into a directory on your hard drive.



Simple, Two-step CORE Generation Process

Pre-Verified Logic Plus Layout

Xilinx DSP LogiCORE™ products are parameterized pre-tested, performance verified cores supported by Xilinx. They take advantage of the distributed RAM, look-up table logic, and segmented routing available in Xilinx devices. Performance is known before the design is implemented.



SDA FIR filter schematic symbol.

Unlike the fixed architecture of DSP processors LogiCORE products are highly parameterized. For example, the SDA FIR filter core can produce over 21 million different filters (not counting the different coefficients). This high level of parameterization is achieved by allowing you to specify characteristics such as sample data, coefficient and output bit widths plus the number of taps and the type of symmetry.

All of the CORE Generator cores come with a physical layout. Relative placement information is included in the netlist. Performance can be maintained independent of how many cores are connected together in the final design and because the placement information is relative, the core can be placed anywhere in a large device.

The XC40125 contains up to 18,496 bytes of SelectRAM memory that can be configured through the CORE Generator to implement multiple FIFOs, dual port RAMs, or shift registers (sample data buffers). Just enter the parameters to specify the width and depth of the memory or FIFO and an optimal design and layout is automatically generated.

Multiplier designs are highly optimized for variable-times-variable or a variable-times-constant using the 16 x 1 look-up table primitive and carry-look-ahead logic.

FFT/DFT algorithms use distributed arithmetic to leverage distributed memory for fast conversion times and minimal device sizes. For example a 1024-point transform will fit in a 13K gate XC4013E but requires a 100K gate part in competing technologies. Basic transform cores can be combined to implement larger transforms, inverse transforms or complex input data transforms.

Xilinx DSP LogiCOREs

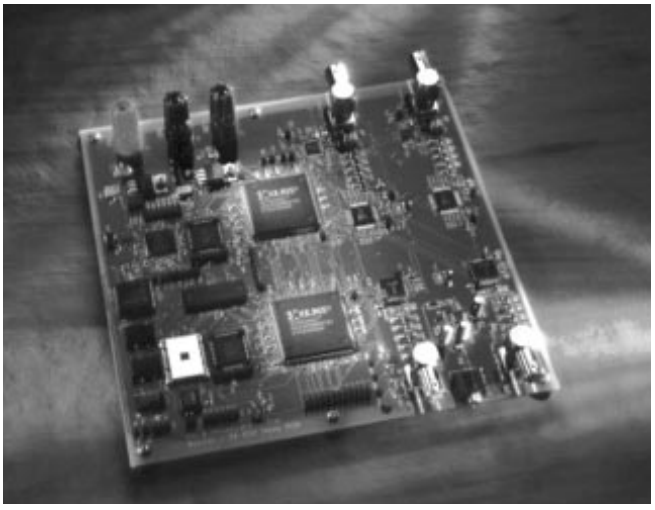
Category	Core	Description	Comments
Filters	SDA FIR Filter	Serial Distributed Arithmetic tap-parallel, bit-serial	Cascadable – any number of taps Symmetrical, non-symmetrical
	Dual channel SDA FIR	Share resources for 2 channels	Supports multi-rate decimation and interpolation.
	PDA FIR Filter	Parallel Distributed Arithmetic Tap-parallel, bit-parallel	
	Comb Filter	Multiplier-less filter	Hogenauer building block
Correlators	RAM-Based Correlator	One dimensional parallel or serial input & output	Combine two cores to build 2-dimensional correlator Efficient, fast
	ROM-Based Correlator		
Building Blocks	Sine/Cosine/Arctan Look-up Table	Expands 90 degree table to 360 degrees	Any bit-width, any table depth
	Time Skew Buffer	RAM-based shift register	Uses 16 by 1 RAM primitive
Memory	FIFOs	Single or dual port	Uses XC4000 distributed 16 x 1 RAM primitives. Produces ideal layout for density and speed. Any width, any depth
	ROM	Look-up table logic	
	RAM	Single or dual port	
Math	Accumulators, Adders/Subtracters, 1's or 2's Complement, Divide		Any bit-width
Multipliers	KCM	Constant times variable	Combinatorial or pipelined
	Area Optimized	Variable times variable	Efficient, fast, highly optimized
	Speed Optimized		
Transforms	FFT 1024-Point	16-bit real input, complex data out	Combine cores to implement inverse transforms, faster and larger transforms.
	DFT 32-, 64-, 128-Point	Internal input buffer	
Other	Cordic	N-bit word	New result every clock
	Square Root	N-bit word	Parameterized output accuracy
	Integrator	Parameterized input and output bit-width Any bit-width	NCO or Hogenauer building block
Basic	Multiplexer, Constant Parallel to Serial Converter Register		Build new cores out of parameterized cores

All Xilinx FPGAs are available in a variety of package types with multiple devices in pin-compatible packages. This allows you to easily upgrade your design to a higher capacity device without changing pinout or changing your PC board.

Xilinx AllianceCORE™

In addition to our own LogiCORE products, Xilinx has partnered with leading third party core providers through the Xilinx AllianceCORE program. This expands the number of complex functions that have been designed, tested, and characterized in Xilinx FPGAs. Our AllianceCORE partners can also customize designs or offer services to help implement specific DSP applications. More information on the AllianceCORE program can be found in the Xilinx CORE Solutions Data Book or on the Xilinx web site at:

http://www.xilinx.com/products/logicore/alliance/tblpart.htm



Xilinx DSP development board contains two analog channels, two Xilinx FPGAs, and one TI 320C54 series DSP processor. Available from AllianceCORE partner.

New Xilinx DSP Programmable Solution. Differentiate Your Product

Summary

Take advantage of the Xilinx programmable DSP solution that can increase the performance of DSP processors 10 to 100 times at 1/5th the cost. With Xilinx HardWire devices, you can convert to a custom silicon solution without putting an extra burden on your engineers. Use Xilinx devices with their unique architectural features including segmented routing, and distributed RAM to boost the power of your DSP processor. Add an FPGA, not more processors!

The Xilinx CORE Generator is available now, on request from your local Xilinx sales office at no charge. LogiCORE and AllianceCORE data sheets are accessible on the web at :

http://www.xilinx.com/products/logicore/tblcores.htm

Xilinx DSP Features

•Performance!	100 million samples per second, more taps
•Lower Cost	1/5th the cost per million MACs
•Distributed RAM	Required for distributed arithmetic, adaptive filters
•Segmented Routing	Superior predictability, lower power, allows higher performance
•HardWire Migration Path	Fastest route to lowest cost silicon with HardWire (FpgASIC)
•CORE Generator	Parameterized cores, logic plus physical layout, VHDL, Verilog, and schematic partners
•DSP AllianceCORE Products	Cores and boards from Xilinx partners
•DSP LogiCORE Products	Xilinx generated and Xilinx-supported cores
• Co-processor	Works with standard DSP processors