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Spartan-II Memory Controller For QDR SRAMs Customer Tutorial

Free VHDL Code

February 2000

SPARTAN-II
FPGA

Agenda

- ◆ Introduction

- ◆ Concept

- ◆ QDR Architecture Advantages

- ◆ Benefits of Using Spartan-II FPGAs to Xilinx Customers

- ◆ Spartan-II FPGAs
  - — The First Memory Controller Solution For QDR SRAM

QDR™ SRAMs

◆ Quad Data Rate (QDR) SRAM

— High-performance SRAM architecture

— Targeted for next generation high speed datacom applications

– Switches and routers operating at data rates above 200 MHz

— Significantly increases memory bandwidth

◆ New Architecture Developed By Cypress, IDT And Micron

— May be adopted by other SRAM vendors

Spartan-II Family

◆ Spartan-II FPGAs As An Ideal Memory Controller Solution
   — 100,000 system gates at under $10
   — Extensive features: BlockRAM, DLL, SelectIO (HSTL)
   — Vast IP portfolio
   — Provide Density, Features, Performance at ASIC prices
   — Reprogrammability

Spartan-II FPGAs Are The First Memory Controller Solution For QDR SRAMs

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Evolution Of Synchronous SRAMs

- ◆ Pipelined-Burst SRAMs (PBSRAM)
  - — Designed for use as a L2 cache for processors
  - — Optimized for long bursts of Reads or Writes
  - — Requires idle cycles to turn bus around in intermixed Read and Write applications

- ◆ Zero-bus-turnaround (ZBT) and No-bus-latency (NoBL) SRAMs
  - — Designed for use in Communications Systems

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Evolution Of Synchronous SRAMs

- ◆ **ZBT and NoBL SRAMs**
  - — Maximizes system bandwidth by eliminating idle cycles in intermixed Read and Write applications
  - — Provides 100% bus utilization
  - — Allows for common I/O bus to be turned around in 1 bus cycle
  - — 3.3V or 2.5V standard LVTTL I/Os
  - — Defined roadmap
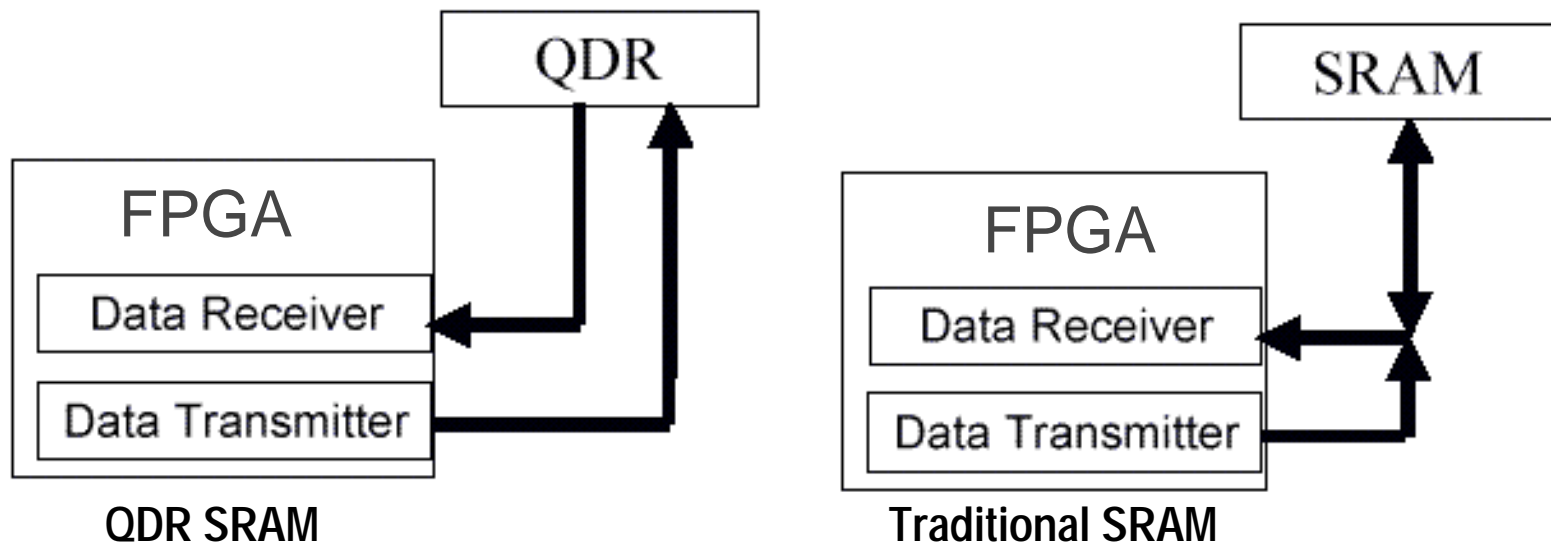   - – 4Mb to 64Mb densities
    - – Up to 200MHz Pipeline

- ◆ **Quad Data Rate (QDR) SRAM**
  - — High-performance SRAM architecture
  - — Targeted for next generation high speed datacom applications

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QDR™ SRAMs

- ◆ Quad Data Rate (QDR) SRAM
  - — Next generation high-performance SRAM architecture
  - — Two ports independently run at Double Data Rate (DDR), resulting in four data items per clock cycle
  - — Targeted for next generation high speed datacom applications
    - – Switches and routers operating at data rates above 200 MHz
  - — Significantly increases memory bandwidth
  - — Will serve as the main memory for look-up tables, linked lists and controller buffer memory
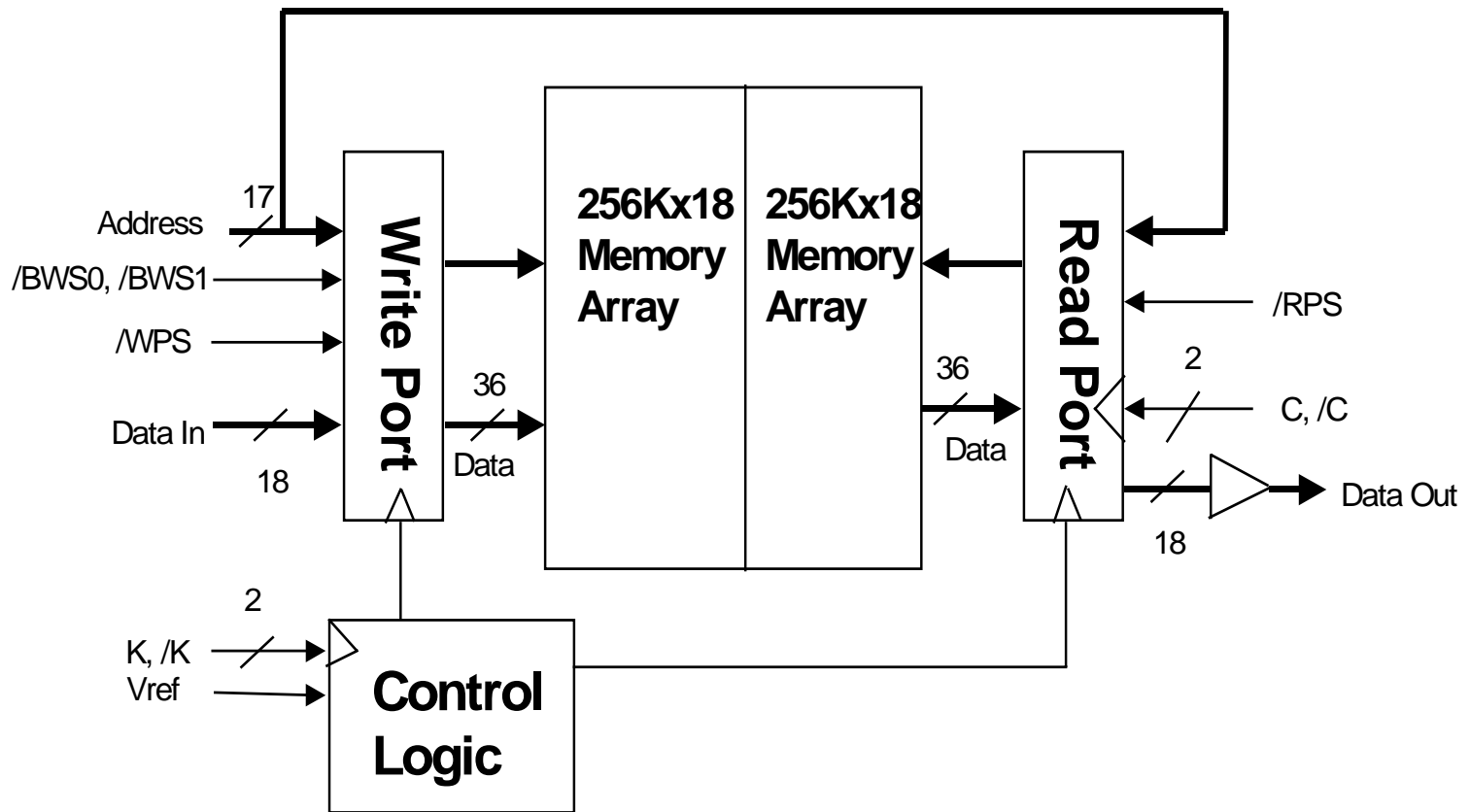
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QDR Simplifies High Speed Design

◆ Separate Inputs and Outputs on QDR SRAMs
  — Remove possibility of bus contention and simplify designs
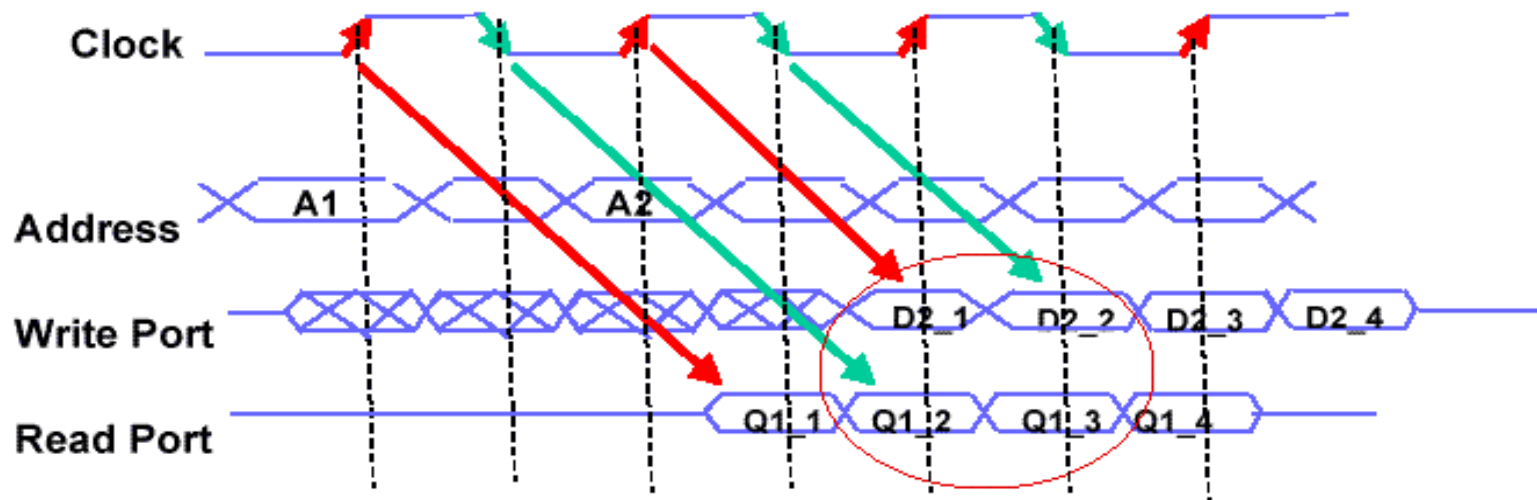 — Facilitate high frequency design

QDR SRAM

Traditional SRAM

(Courtesy: QDR Consortium)

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QDR SRAM Block Diagram

Address — 17

/BWS0, /BWS1

/WPS

Data In — 18

Write Port

36
Data

256Kx18 Memory Array

256Kx18 Memory Array

36
Data

Read Port

/RPS

2
C, /C

Data Out
18

K, /K — 2
Vref

Control Logic

(Courtesy: Cypress Semiconductor)

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QDR Simplified Timing Diagram

- ◆ Separate I/O
  - — Separate DDR Read and Write Ports

- ◆ Simultaneous Read and Write
  - — DDR on two ports provides four data items per clock or Quad Data Rate

Clock	

Clock

Address — A1 — A2

Write Port — D2_1 — D2_2 — D2_3 — D2_4

Read Port — Q1_1 — Q1_2 — Q1_3 — Q1_4

(Courtesy: QDR Consortium)

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QDR Architecture Advantages

◆ Separate I/O

— Separate input & output ports

— Bus contention

– Occurs frequently in a networking environments

– Occurs when the SRAM drives the data on a read faster than the ASSP can take data off the bus after a write

– As operating frequencies increase, bus contention rises dramatically

– Separating read & write data buses ensures that bus contention never occurs

— Constant flow of data

– Requires the bus be turned around for a read & write

– Causes non-uniform data flow between controller & SRAM

– QDRs provide a higher throughput than common SRAMs

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QDR Architecture Advantages

◆ **Maximum Frequency/Bandwidth**
  — PB-, ZBT- & NoBL SRAMs can run at very high frequencies
    – But limited due of operating a common I/O data path
  — Double Data Rate transfers on both input and output ports
    – Improves throughput through simultaneous read and write

◆ **Voltage Migration**
  — I/O pins of QDR SRAMs operate at HSTL voltage levels
    – At lower voltage levels, there is low-swing, high-speed operation of the inputs and outputs
   – Easy migration to lower voltage levels

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Spartan-II QDR SRAM Benefits

- ◆ QDR is Expected to be the Most Widely Accepted High-Bandwidth SRAM Architecture of the Future
  - — Top-10 Datacom customers have committed to using QDR
  - — Other Customers are evaluating the use of QDR SRAMs

- ◆ Xilinx has the only Memory Controller Solution for this Next Generation SRAM Today
  - — Spartan-II and future derivatives through performance and features will be used as memory controllers in advanced networking architectures

VHDL Code Available Free From Xilinx Website

Spartan-II QDR SRAM Controller

Free VHDL Code
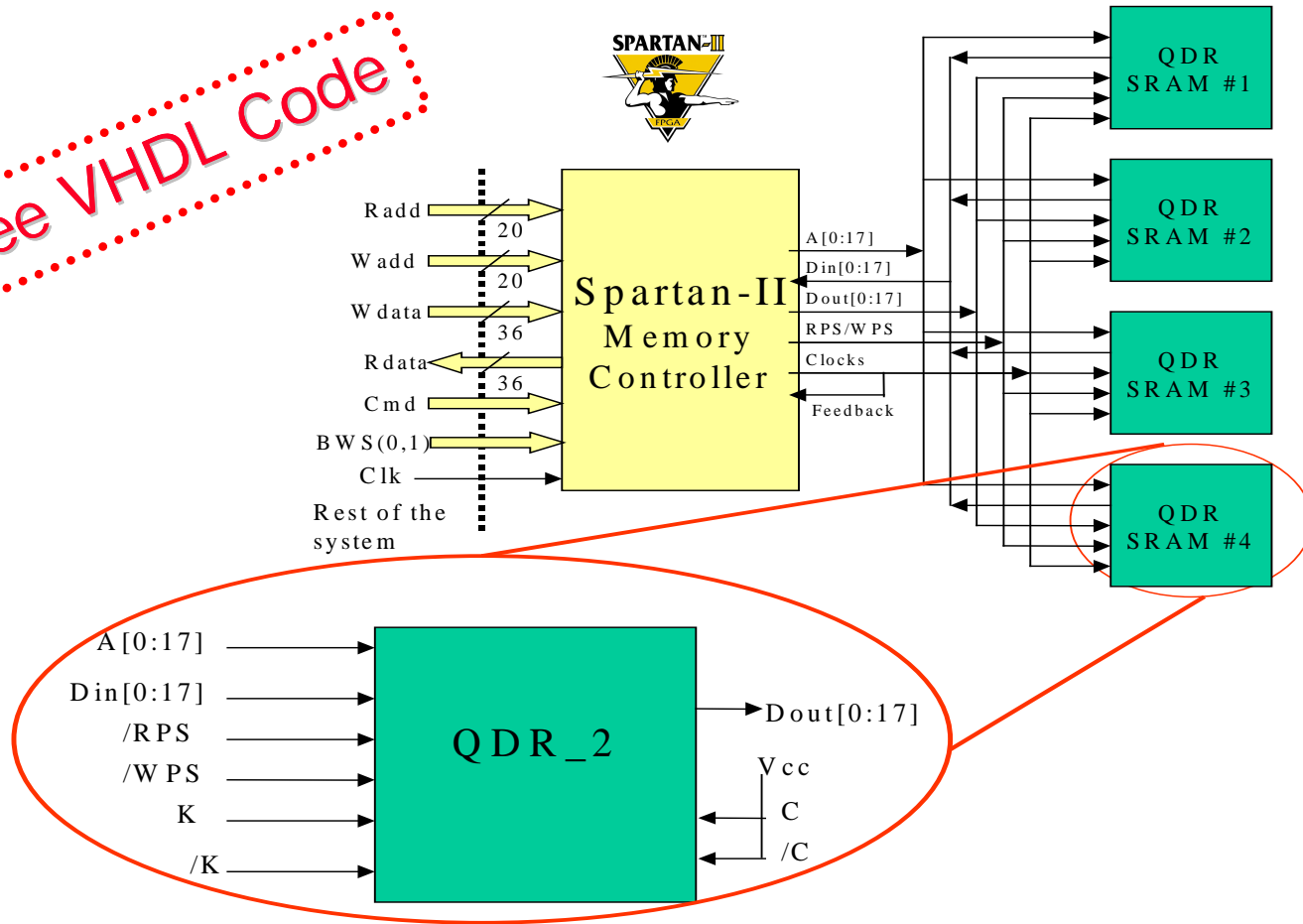
VHDL code available for free download from www.xilinx.com

The Spartan-II Competitive Advantage

- ◆ First and Only Memory Controller Solution for QDR SRAM

- ◆ VHDL Available for Free Download from Xilinx Website

- ◆ Spartan-II Advantage
  - — High-Speed Transceiver Logic (HSTL) I/O Buffers
  - — Delay-Locked Loops (DLL)
  - — Block SelectRAM
  - — I/O Performance
  - — Core Performance
  - — Availability (first & only solution)

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