Quad Data Rate™ SRAM

QDR™

QDR RAMs and Quad Data Rate comprise a new family of products developed by Cypress Semiconductor, IDT, Inc. and Micron Technology

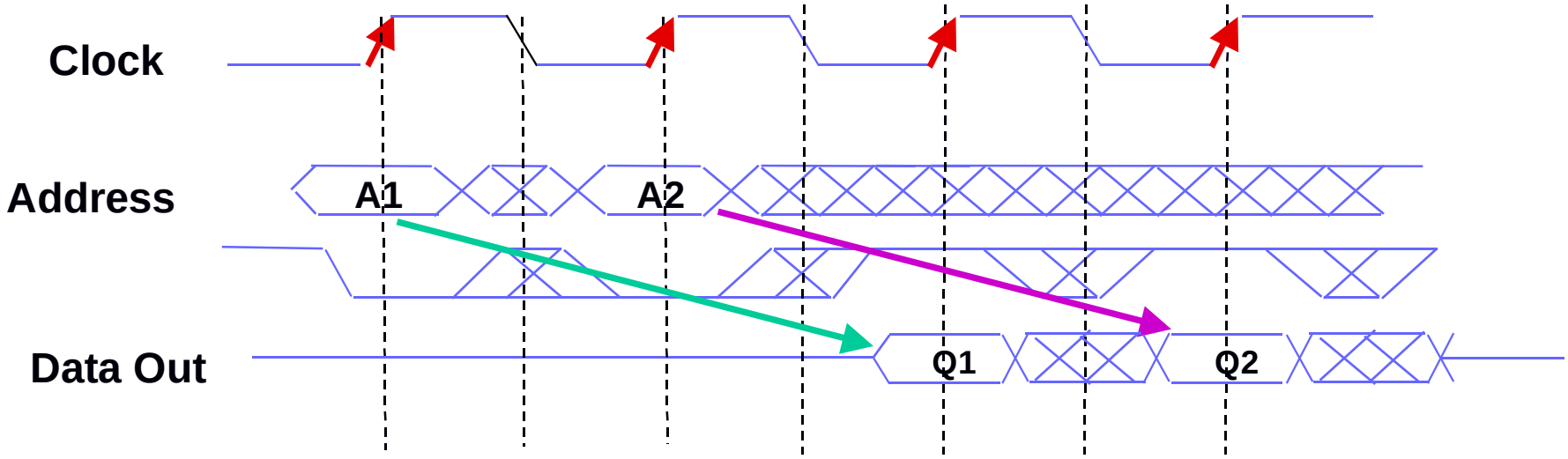
Evolution of Synchronous SRAM

- PBSRAMs were designed for use as an L2 cache for processors
  - Optimized for long bursts of Reads or Writes
  - Requires idle cycles to turn bus around in intermixed Read and Write applications
- ZBT and NoBL were designed for use in communications systems
  - Maximizes system bandwidth by eliminating idle cycles in intermixed Read and Write applications
  - Provides 100% bus utilization
  - Allows for common I/O bus to be turned around in 1 bus cycle

ZBT and NoBL

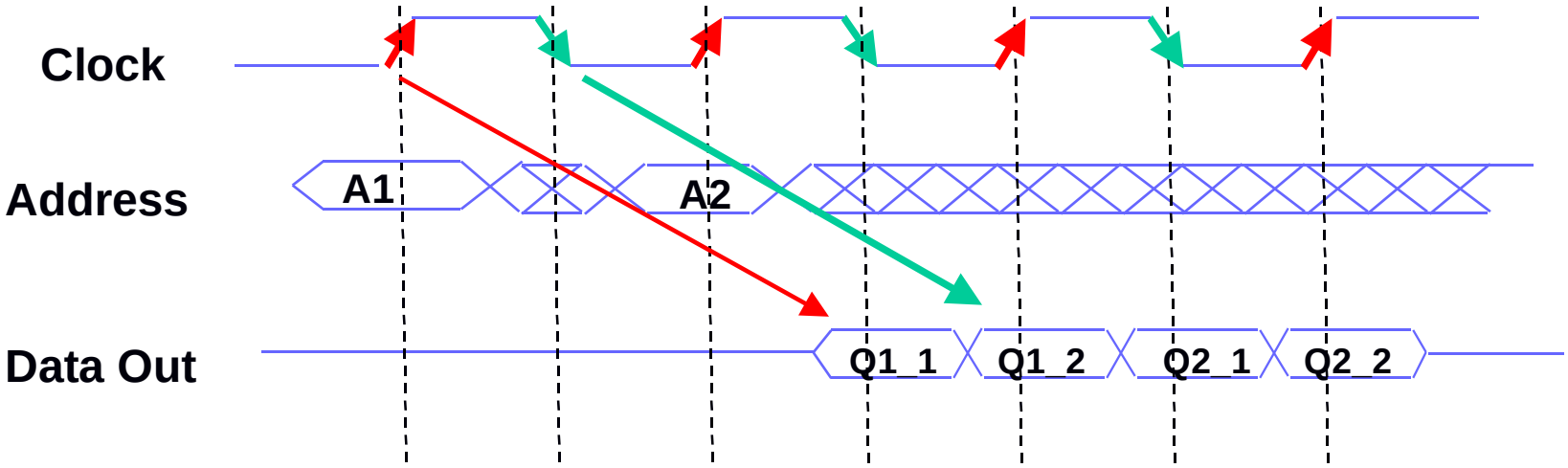
- Compatible with the ASICs and Processors used in today's communications systems
  - 3.3V or 2.5V standard LVTTL I/Os
- Defined roadmap
  - 4Mb to 64Mb densities
  - Up to 200MHz Pipeline

Single Data Rate



- One data item per Address
- One data item per Clock cycle
- Common data bus for Inputs and Outputs

Double Data Rate



- Two data items per Address
- Two data items per Clock cycle
  - One data item on Clock rising edge and one data item on Clock falling edge
- Common data bus for Inputs and Outputs
- Allows only 1/2 the time for bus turnaround compared to single data rate

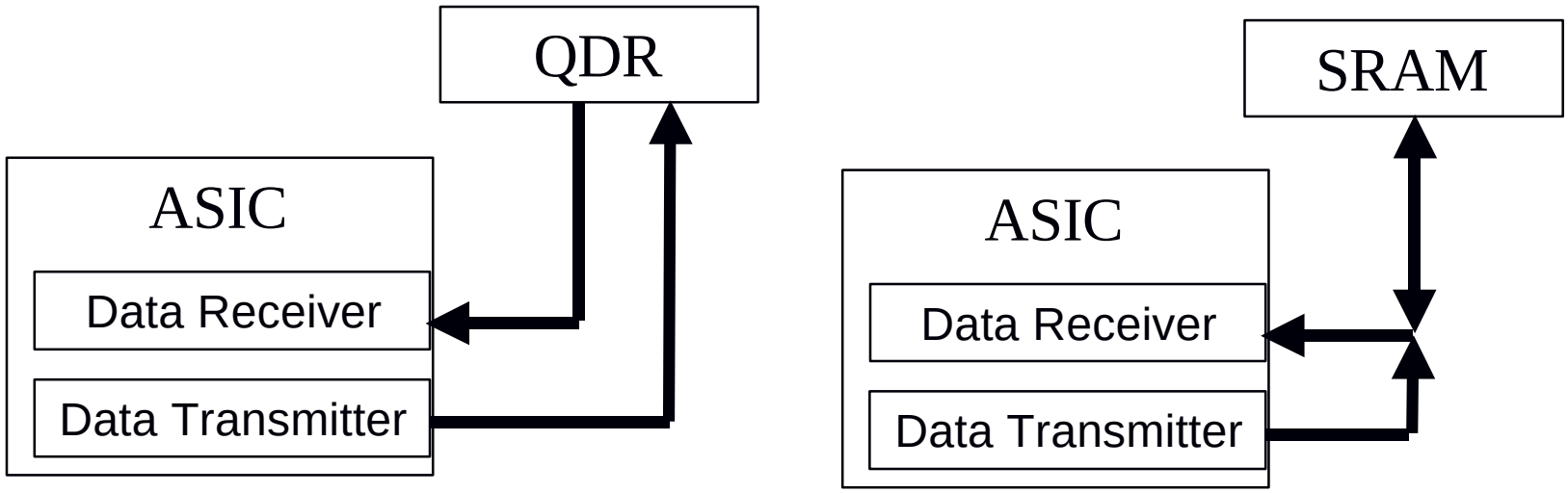
Future Requirements

- Higher system bandwidth required
- Utilize standard interfaces
- Provide a migration path for future growth
- Provide multiple sources
- Resolve issue of bus turnaround at higher frequencies

QDR

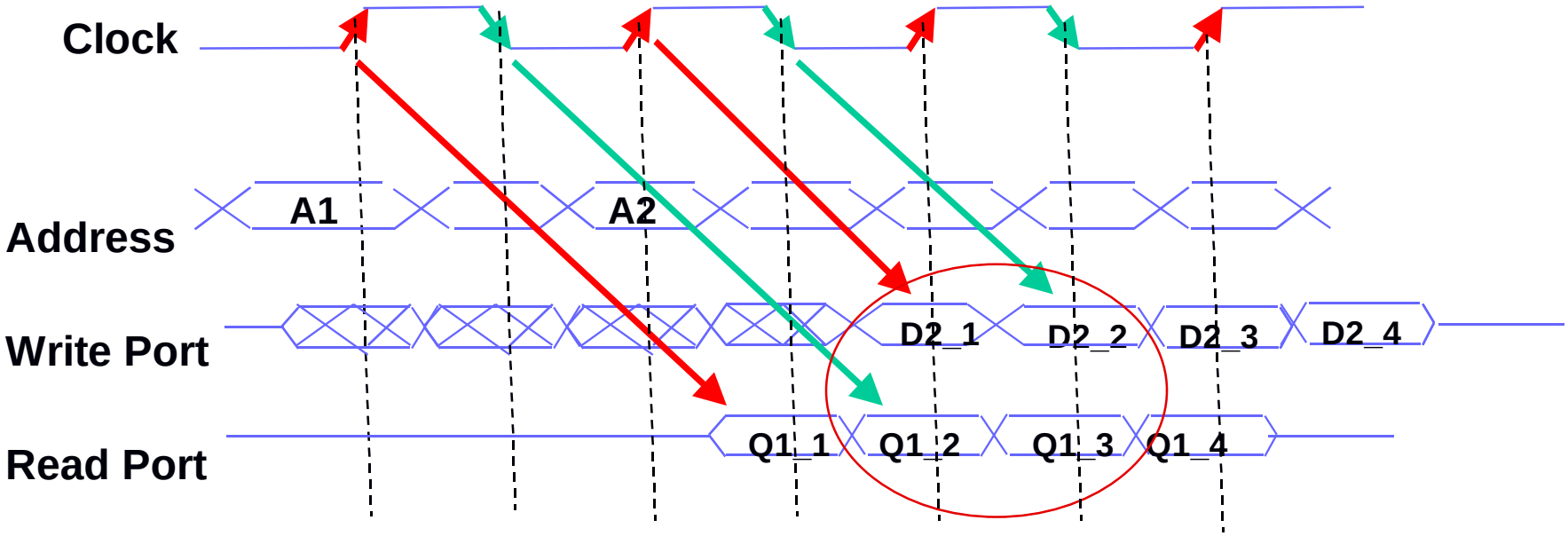
Cypress, IDT, and Micron introduce QDR

QDR Simplifies High Speed Design



- Separate Input and Output on QDR removes possibility of bus contention
- Unidirectional busses simplify design
  - Facilitates high frequency design

Quad Data Rate



- Separate I/O
  - Separate Double Data Rate Read and Write Ports
- Simultaneous Read and Write
  - Double Data Rate on two ports provides four data items per clock or Quad Data Rate

QDR Roadmap

- Multiple sources
  - Joint development between Cypress, IDT and Micron
- 9Mb initial density
  - Pinout migration to 64Mb
- 167MHz Clock frequency (333MHz Data Rate)
  - Migration to 250MHz Clock frequency (500MHz Data Rate)
- First devices from QDR consortium expected in calendar 4Q99

Data Transactions Summary

- Single Data Rate
  - One data item per Clock cycle
  - Allows for single data transaction Reads or Writes
- Double Data Rate
  - Two data items per Clock cycle
  - Requires burst of two data transactions per Read or Write
- QDR
  - Four data items per Clock cycle
  - Bursting of data required

Why ZBT or NoBL?

- SRAM standards for communications market
  - Compatible with today's systems
  - 3.3V or 2.5V standard LVTTL I/Os
- For today's system requirements of 66MHz to 200MHz data rates
- Defined migration from 4Mb to 64Mb
- Flexibility of data structure
  - No burst requirement

Why QDR?

- For new designs requiring greater than 200MHz data rates
  - Separate I/O eliminates possibility of bus contention
- High speed clocking scheme minimizes skew

Summary

- ZBT and NoBL provide high bandwidth solutions for designs up to 200MHz data rates
- QDR provides a multiple-sourced solution for designs beyond 200MHz data rates
  - Simultaneous DDR Read and Write provides Quad Data Rate
  - Separate I/O eliminates bus contention