XF-TWSI Two-Wire Serial Interface Master

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Features

- Supports 4000X, Spartan, Spartan™-II, Virtex™, and Virtex™-E devices
- I²C-compatible two-wire serial interface core; *I²C is a trademark of Philips, Inc*.
- Compatible with Xilinx CORE Generator tool
  - Xilinx netlist version available on enCORE CD-ROM
- Multi-master operation with arbitration and clock synchronization
- Support for reads, writes, burst reads, burst writes, and repeated start
- User-defined timing and clock frequency
- Fast mode and standard mode operation
- Compatible with popular protocols

Applications

- Embedded microprocessor boards
- Consumer and professional audio/video
- Home and automotive radio

AllianceCORE™ Facts		
Core Specifics		
Device Family	XC4000E/XL	Spartan
CLBs Used		
Core	102	97
Core+Ext logic	102	97
Core I/O		
Core[1]	32	32
Core+Ext logic	30	30
System Clock f_{max}	10+ MHz[2]	
Device Features Used	Tbufs, global clock buffers	
Provided with Core		
Documentation	User's guide, Application notes, Implementation instructions	
Design File Formats	.ngo netlist	
Constraint Files	.ucf	
Verification Tool	Testbench for VHDL	
Symbols	VHDL	
Evaluation Model	None	
Reference designs & Application notes	Sample design in Verilog	
Additional Items	Warranty by MDS Netlist only version available on enCORE CD-ROM	
Design Tool Requirements		
Xilinx Core Tools	Alliance/Foundation 1.4	
Support		
Support provided by Memec Design Services.		

Notes:
1. Assuming all core signals are routed off-chip.
2. Minimum guaranteed speed.

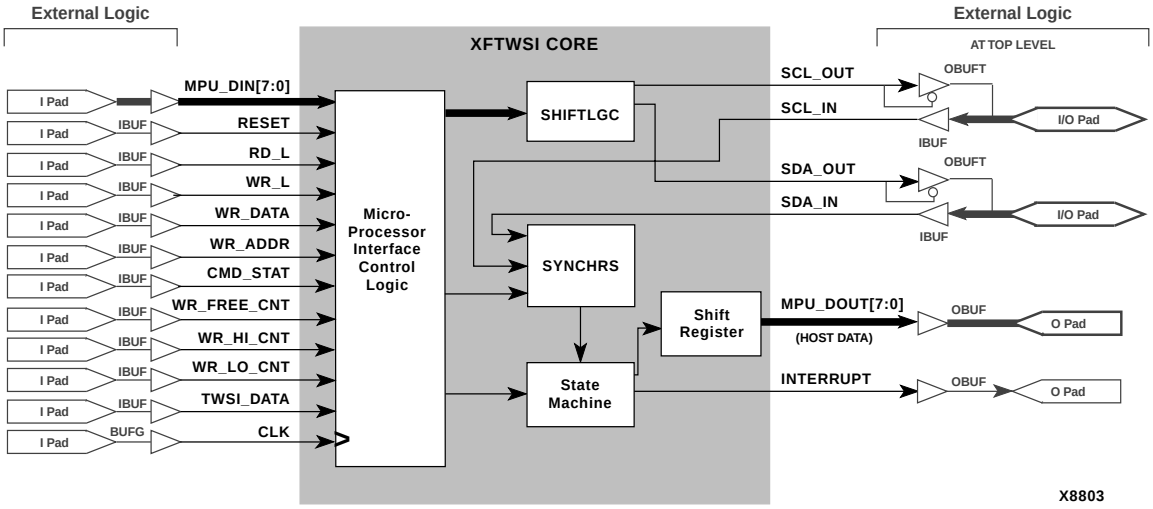

Figure 1: XF-TWSI Block Diagram

General Description

The XF-TWSI is a "core" logic module specifically designed for Xilinx FPGAs that provides the functionality of the industry standard two-wire serial interface supporting multiple masters. This core is master only; it is not a slave. This core does not support General Call Addressing, 10-bit slave addressing, or START byte data transfers. It facilitates upgrading current systems by allowing the designer to incorporate the XF-TWSI function as well as other logic into a single, state of the art FPGA.

MDS cores are designed with the philosophy that no global elements should be embedded within the core itself. Global elements include any of the following components: STARTUP, STARTBUF, BSCAN, READBACK, Global Buffers, Fast Output Primitives, IOB Elements, Clock Delay Components, and any of the Oscillator Macros. MDS cores only contain resources present in the CLB array. This is done to allow flexibility in using the cores with other logic. For instance, if a global clock buffer is embedded within the core, but some external logic also requires that same clock, then an additional global buffer would have to be used.

In any instance, where one of our cores generates a clock, that signal is brought out of the core, run through a global buffer, and then brought back into the core. This philosophy allows external logic to use that clock without using another global buffer.

A result of this philosophy is that the cores are not self-contained. External logic must be connected to the core inorder to complete it. MDS cores include tested sample designs that add the external logic required to complete the functionality. This datasheet describes both the core and the supplied external logic.

The Absolute Maximum Ratings, Operating Conditions, DC Electrical Specifications, and Capacitance are device dependent and can be found in the Xilinx datasheet for the target device.

Functional Description

The XF-TWSI is partitioned into modules as shown in Figure 1 and described below. Refer to XF-TWSI User's Guide for detailed technical information. The User's Guide is available, directly from MDS.

Microprocessor Interface Control Logic

There are three registers used to interface to the host: the Data Register, the Address Register, and the Command Register. The strobes WR_DATA, WR_ADDR, and CMD_STAT are directly connected to the clock enable pins of these register flip-flops for ease of interface.

Shift Logic

The basic cycle on the XF-TWSI serial interface consists of an address cycle followed by a data cycle. The address consists of seven bits and the read/write bit (the LSB). The MSB is always transmitted first on the SDA line. The data cycle can either be a read or a write. For a write operation the macro shifts the data from the Data Register onto the SDA line. For a read operation the macro captures the data into the Shift Register. The data cycle can end in three different ways:

1. A stop can be generated which terminates the current cycle.

2. Another data cycle can take place (a burst).
3. A repeated start can be generated by the interface.

There is always one interrupt generated for each data cycle, independent of the type of cycle. For example, for a burst read cycle an interrupt will be generated for each byte read. For a burst write cycle an interrupt will be generated when each byte transfer is completed.

A repeated start is used to turn the bus around; when a read cycle must be followed directly by a write cycle without a stop in-between. Since the READ bit is a part of the address, if a read followed by write is desired without a stop command, a second address must be issued following the data cycle. The sequence of events in a repeated start cycle is: start, address cycle, data cycle, repeated start, address cycle, data cycle, stop. If bursting is desired, each of the data cycles can be repeated. And if desired, the stop cycle could be another repeated start.

Synchrs

The SDA and SCL inputs are passed through this module that performs a dual-rank synchronization and glitch filtering when enabled by the FILTER_EN signal. The synchronized versions of the SDA and SCL signals are used in all macro modules.

The XF-TWSI core treats both the SDA and SCL lines as data lines. The SDA line is actually sampled some number of clocks after the rising edge of SCL is detected. This allows for greater noise immunity and more robust operation.

State Machine

The control for the serial interface comes from the TWSI_SM state machine. This state machine controls the loading and enabling of all shift registers and counters, and is responsible for implementing the basic interface protocol.

Shift Register

There is a single parallel-in, parallel-out, serial-in, serial-out shift register called NUPSHIFT, which performs the shifting of data for address cycles, write cycles, and read cycles. The parallel output drives the macro interface pins MPU_DOUT which are used to return read data to the host.

Core Modifications

Implementation beyond 10MHz and other customizing is available through Memec Design Services.

Pinout

The XF-TWSI may be implemented as stand-alone logic or may be implemented internally with the user's design. Both versions are included with the Core deliverables. Signal names are provided in the block diagram shown in Figure 1and Table 1.

Verification Methods

Complete functional and timing simulation has been performed on the XF-TWSI using ModelSim. (Simulation vectors used for verification are provided with the core.). This core has also been used successfully in customer designs.

Recommended Design Experience

For the source version, users should be familiar with VHDL simulation/synthesis and Xilinx design flows. For the netlist version, users should be familiar with Workview office, Xilinx Foundation, or VHDL simulation/synthesis. Users should also have experience with microprocessor systems.

Ordering Information

The XF-TWSI Two Wire Serial Interface Core is provided under license from Memec Design Services for use in Xilinx programmable logic devices and Xilinx HardWire gate arrays. Please contact Memec for pricing and more information.

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
MPU_DIN[7:0]	Input	Microprocessor Data In lines; used to program Data, Address, and Command Registers.
RESET	Input	Reset; active high.
RD_L	Input	Allows reads on MPU_DOUT when active "0" with proper read buffer/register is selected.
WR_L	Input	Rising edge of this signal registers data in internal registers when proper address is selected.
WR_DATA	Input	When active "1" with WR_L strobes 8 Bits from MPU_DIN into Data Register for serial bus write cycle.
WR_ADDR	Input	When active "1" with WR_L strobes least significant 7 Bits of MPU_DIN into Address Register for all Serial Bus Operations.
CMD_STAT	Input	When active "1" with WR_L strobes least significant 5 Bits from MPU_DIN into Command Register, initiates serial bus cycle and clears the Interrupt line. When active "1" with RD_L reads status register.
WR_FREE_CNT	Input	When active "1" with WR_L strobes 8-bits from MPU_DIN into the BUSFREE_COUNT register, used to set the bus free period.
WR_HI_CNT	Input	When active "1" with WR_L strobes 8-bits from MPU_DIN into HI_COUNT register, used to set number of CLK clock periods for low period of SCL and setup time for repeated start operation.
WR_LO_CNT	Input	When active "1" with WR_L strobes 8Bits from the MPU_DIN into LO_COUNT register used to set number of CLK clock periods for high count of SCL, hold time for start command, and setup time for stop command.

Table 1: Core Signal Pinout (cont)

Signal	Signal Direction	Description
TWSI_DATA	Input	Allows reads on MPU_DOUT when active "1" with RD_L.
CLK	Input	Primary clock.
SCL_OUT	Output	Serial clock with open collector output.
SCL_IN	Input	Serial clock with open collector input.
SDA_OUT	Output	Serial data with open collector output.
SDA_IN	Input	Serial data with open collector input.
MPU_DOUT[7:0]	Output	Returns read data after activation of Interrupt pin and error free status; lower three bits are also Status Register.
INTERRUPT	Output	Interrupt line set upon completion or abort of serial cycle; active high.

Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
2100 Logic Drive
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Phone: +1 408-559-7778
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For general Xilinx literature, contact:

Phone: +1 800-231-3386 (inside the US)
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For AllianceCORE™ specific information, contact:

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URL: www.xilinx.com/products
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