XF8256 Multifunction Microprocessor Support Controller

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Features

- Compatible with Xilinx CORE Generator tool
- Programmable serial asynchronous communications interface for 5-, 6-, 7-, or 8-bit characters, 0.75, 1, 1.5, or 2 stop bits, and parity generation
- On-board baud rate generator programmable for 13 common baud rates up to 19.2 K bits/second, or an external baud clock maximum of 1M bit/second
- Five 8-bit programmable timer/counters; four can be cascaded to two 16-bit timer/counters
- Two 8-bit programmable parallel I/O ports; port 1 can be programmed for port 2 handshake controls and event counter input
- Eight-level priority interrupt controller programmable for 8085, 8086/88, 80186/188 systems and for fully nested interrupt capability
- Programmable system clock to 1x, 2x, 3x, or 5x 1.024 MHz

Applications

- Serial communications
- Process control
- Embedded systems

AllianceCORE™ Facts

Core Specifics		
Device Family	XC4000E/XL	Spartan
CLBs Used		
Core	354	354
Core+Ext logic	354	354
Core I/O		
Core[1]	77	77
Core+Ext logic	38	38
System Clock f_{max}	10+ MHz[2]	
Device Features Used	Tbufs, global clock buffers	
Provided with Core		
Documentation	User's guide, Application note and Implementation instructions	
Design File Formats	.ngo netlist Viewlogic source files available extra	
Constraint Files	.ucf	
Verification Tool	Machine-readable simulation vectors for ViewLogic ViewSim, Testbench for VHDL and Verilog	
Symbols	ViewLogic, Foundation Instantiation templates for VHDL and Verilog	
Evaluation Model	None	
Reference designs & application notes	Sample designs in Viewlogic, Foundation, VHDL and Verilog.	
Additional Items	Warranty by MDS Netlist only version available on enCORE CD-ROM.	
Design Tool Requirements		
Xilinx Core Tools	Alliance/Foundation 1.4	
Support		
Support provided by Memec Design Services.		

Notes:
1. Assuming all core signals are routed off-chip.
2. Minimum guaranteed speed.

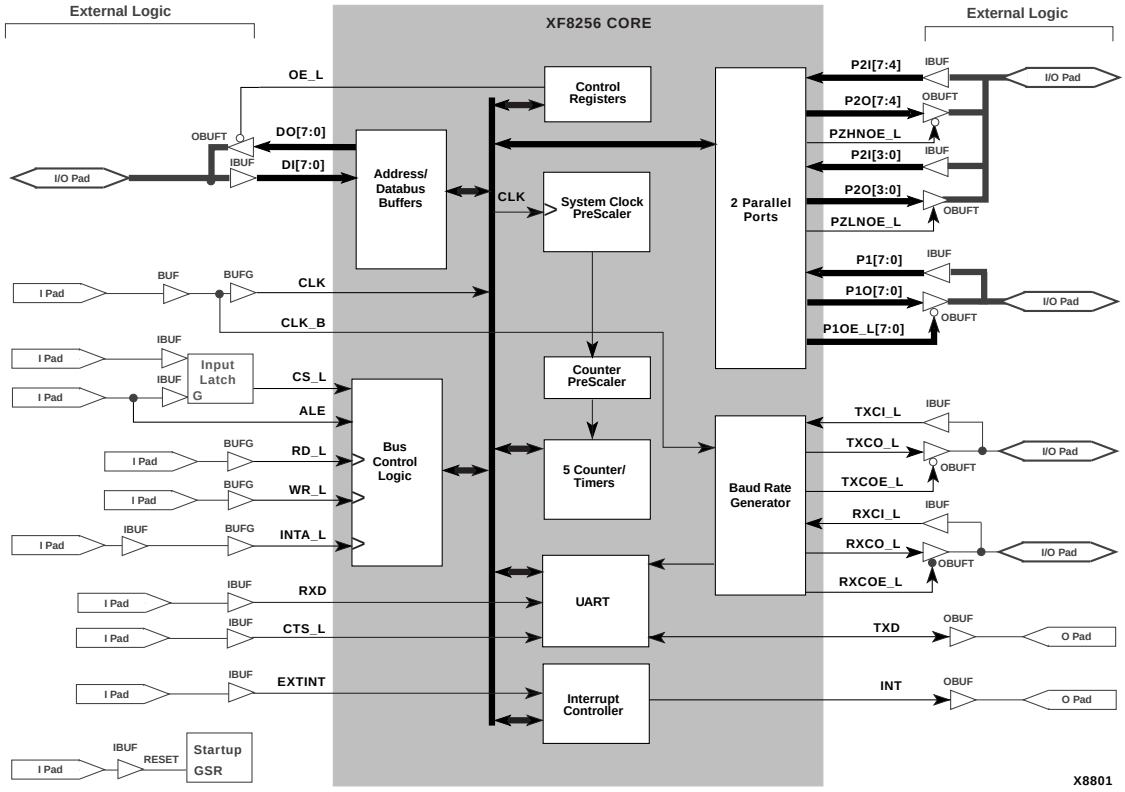

Figure 1: XF8256 Multifunction Microprocessor Support Controller Block Diagram

General Description

The XF8256 Multifunction Microprocessor Support Controller combines five commonly used functions into a single device: serial communications, parallel I/O, timing, event counting, and priority interrupt functions.

It is designed to interface with the 8085, 8086/88, 80186/188, and 8051. All of these functions are fully programmable through internal registers. In addition, the five counter/timers and two parallel I/O ports can be accessed directly by the microprocessor as shown in Figure 1.

MDS cores are designed with the philosophy that no global elements should be embedded within the core itself. Global elements include any of the following components: STARTUP, STARTBUF, BSCAN, READBACK, Global Buffers, Fast Output Primitives, IOB Elements, Clock Delay Components, and any of the Oscillator Macros. MDS cores only contain resources present in the CLB array. This is done to allow flexibility in using the cores with other logic. For instance, if a global clock buffer is embedded within the core, but some external logic also requires that same clock, then an additional global buffer would have to be used.

In any instance, where one of our cores generates a clock, that signal is brought out of the core, run through a global buffer, and then brought back into the core. This philosophy allows external logic to use that clock without using another global buffer.

A result of this philosophy is that the cores are not self-contained. External logic must be connected to the core in order to complete it. MDS cores include tested sample designs that add the external logic required to complete the functionality. This datasheet describes both the core and the supplied external logic.

Functional Description

The XF8256 core internal structure is shown in Figure 1 and described below.Refer to the XF8250 User's Guide for

detailed technical information. The User's Guide is available directly fromMDS.

Bus Control Logic

This block controsl the movement of data between the host microprocessor and internal blocks of XF8256.

Control Registers

These store commands and input and output data.

System Clock PreScaler

This provides division ratios of 5, 3, 2, or 1 to generate the internal clock operating frequency of 1.024 MHz.

Counter/Timers

Five 8-bit counter/timers are available with either 1 kHz or 16 kHz internally generated clocks. Four of these can be cascaded to two 16-bit counter/timers and one can be reset to its initial value by an external pin.

UART

The UART portion of the XF8256 is a full-duplex receiver and transmitter with 32x or 64x sampling rate. A programmable baud rate generator is included to select a variety of popular speeds without external logic.

The CPU can program character sizes, parity detection and generation, error detection, start and stop bit handling, and baud rate speed. The receiver can be programmed to sample input bits anywhere between the start and end of the bit. The transmitter can send breaks that can be controlled by an external pin. The receiver can halt the reception of data on these breaks.

Interrupt Controller

The XF8256 employs an eight-level priority interrupt controller with fully nested or normal interrupt priority modes.

Seven of the eight interrupt service functions are for the UART and counter/timers. The remaining one is external and can be used for particular functions or for chaining interrupt controllers. The interrupt controller supports 8085/86/88 system interrupt vectoring or it can be polled to determine the cause of the interrupt.

Parallel Ports

Two, 8-bit general purpose parallel ports are available, Port 1 and Port 2. Each bit of Port 1 can be individually defined as input/output, or used for special I/O functions. Port 2 has handshake capability and can be used to handle bytes or nibbles (4 bits).

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
OE_L	Output	Address/data bus output enable.
DO[7:0]	Input	Address/data bus output.
DI[7:0]	Input	**Address/data bus input:** Three-state address/data lines interface to lower 8-bits of microprocessor's multiplexed address/data bus.
CLK	Input	**System clock**: Reference clock from system used to generate internal timing.
CLK_B	Input	System clock input to non-clocked logic.
CS_L	Input	**Chip select**: A low on this pin enables the interface functions to send or receive.
ALE	Input	**Address latch enable**: Latches the address lines on AD[0:4] and CS_L on the falling edge.
RD_L, WR_L	Input	**Read and write control**: These signals enable data buffers to either send or receive data to or from external bus.
INTA_L	Input	**Interrupt acknowledge**: informs core that its interrupt request is being acknowledged by the microprocessor.
RXD	Input	**Receiver data**: Serial data input.
CTS_L	Input	**Clear to send**: This input enables the serial transmitter. It can be level sensitive or edge sensitive.
EXTINT	Input	**External interrupt**: An external device can request interrupt service through this level-sensitive input.
P2I[7:4]	Input	Parallel I/O port 2 upper input nibble.
P2O[7:4]	Output	Parallel I/O port 2 upper output nibble.
PZHNOE_L	Output	Parallel I/O port 2 upper nibble output enable.
P2I[3:0]	Input	Parallel I/O port 2 lower input nibble.
P2O[3:0]	Output	Parallel I/O port 2 lower output nibble.

Table 1: Core Signal Pinout (cont.)

Signal	Signal Direction	Description
PZLNOE_L	Input	Parallel I/O port 2 lower nibble output enable.
P1I[7:0]	Input	Parallel I/O port 1 input.
P1O[7:0]	Output	Parallel I/O port 1 output.
P1OE_L[7:0]	Output	Parallel I/O port 1 output enable.
TXCI_L	Input	Transmitter clock input.
TXCO_L	Output	Transmitter clock output.
TXCOE_L	Output	Transmitter clock output enable.
RXCI_L	Input	Receiver clock input.
RXCO_L	Output	Receiver clock output.
RXCOE_L	Output	Receiver clock output enable.
TXD	Output	**Transmitter data**: Serial data output.
INT	Output	**Interrupt request**: A high signals microprocessor that XF8256 needs interrupt service.

Baud Rate Generator

This block is a programmable baud rate generator with selectable internal or external clock inputs.

Core Modifications

For the source version, the XF8256 can be broken into subfunctions that can be used as needed. Multiple XF8256s can be instantiated into one device to perform functions in parallel. Timing specifications are not critical and can be tightened significantly.

In all cases, a functional and post route timing analysis should be performed to verify performance. Implementation and customizing is available through Memec Design Services.

Pinout

The XF8256 may be implemented internally with the user's design or as stand alone logic. For fast replacement of the industry standard 8256, MDS offers a 40-pin device carrier that is pin compatible. Signal names are provided in the block diagram shown in Figure 1 and described in Table 1.

Verification Methods

Basic functional simulation has been performed on the XF8256 using ViewSim. Simulation vectors used for verification are provided with the core. This FPGA design was also physically tested and compared with the industry standard 8256 for verification purposes.

Available Support Products

Memec Design Services supplies a Xilinx-based FPGA Development Module that can be used to hardware test this and other MDS cores. To purchase this, or obtain more information, contact Memec Design Services.

Recommended Design Experience

For the source code version, users should be familiar with ViewLogic Workview Office schematic entry and Xilinx design flows. For the netlist version, users should be familiar with Workview office, Xilinx Foundation, Verilog simulation/synthesis or VHDL simulation/synthesis.

Ordering Information

The XF8256 Multifunction Microprocessor Support Controller is provided under license from Memec Design Services for use in Xilinx programmable logic devices and Xilinx HardWire™ gate arrays. To purchase or make further inquiries about this or other Memec Design Services products, contact MDS directly at the location listed on the front page.

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Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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