Cell Assembler (CC-201)

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CoreEl MicroSystems

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Features

- Octet-wide operation
- Cell Rate Adaptation
  - Transmission convergence idle cells inserted when input cell not present
  - Fixed idle cell header, HEC, and payload patterns as specified in ATM UNI 3.1
- HEC Computation
  - HEC computed and inserted into the 5th byte of the cell header
  - Coset polynomial always added
- Cell Scrambling
  - Self-synchronizing scrambler as specified in ATM UNI 3.1
  - Does not scramble cell header
- Cell transmitted pulse output
- Continuous clock with cycle-by-cycle enable

Applications

The Cell Assembler core can be used in Asynchronous Transfer Mode (ATM) networking systems such as adapter cards, routers and switches.

AllianceCORE™ Facts

Core Specifics	
Device Family	XC4000XL
CLBs Used	87
IOBs Used	22[1]
System Clock f_{max}	60 MHz
Device Features Used	None

Supported Devices/Resources Remaining		
	I/O	CLBs
XC4005XL-1 PC84	39[1]	109

Provided with Core	
Documentation	Product Brief Specification Document Design Document Test Bench Design Document
Design File Formats	VHDL compiled, EDIF netlist
Constraint Files	UCF File, Exemplar scripts
Verification Tool	Behavioral VHDL Test Bench
Schematic Symbols	None
Evaluation Model	Behavioral VHDL
Reference designs & application notes	ATM-UNI Specification
Additional Items	None

Design Tool Requirements	
Xilinx Core Tools	Alliance 1.3
Entry/Verification Tool	Model Tech V-System

Support
Support provided by CoreEl Microsystems

Note:
1. Assuming all core signals are routed off-chip.

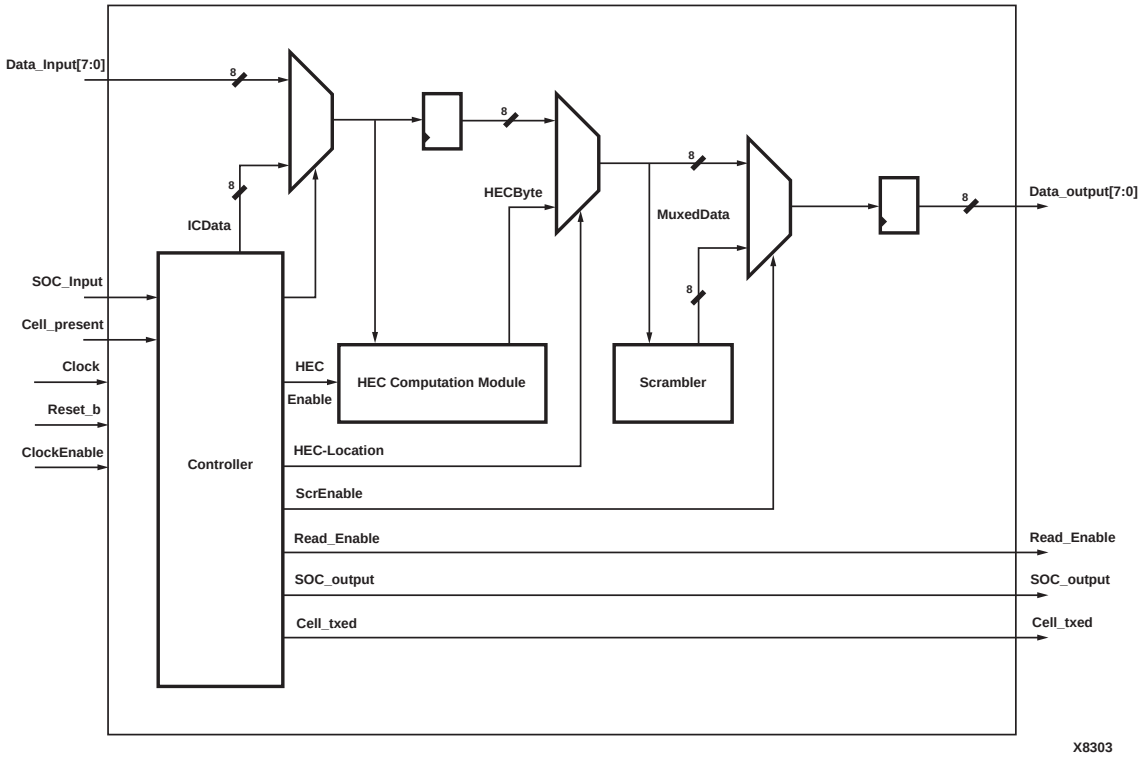

Figure 1: Cell Assembler Core Block Diagram

General Description

The Cell Assembler carries out the functions required to be performed in the receive stream of the Transmission Convergence sub-layer of an ATM Physical Layer processor. The input is a byte-aligned cell stream containing 52-byte cells with 4 bytes of header and 48 bytes of payload. The Cell Assembler computes the header Error Check sequence and inserts it in the fifth byte position of the outgoing stream; thus creating the 53 byte output cell

Functional Description

The Cell Assembler core is divided into blocks as shown in Figure 1: Controller, HEC Computation Module and Scrambler. The Clock, ClockEnable and Reset_b signals are common to all modules.

Controller Block

The Controller inputs SOC_Input and Cell_present signals and controls the data flow. It also inserts idle cells when assigned cells are not present at the input. At the end of every cell, it checks the cell_present signal. If a cell is present, the controller asserts Read_Enable and reads its header. It deasserts Read_Enable for one clock when it insertion of HEC in the stream, the controller reads payload. At the end of the cell it checks the cell present signal again for deciding whether to insert idle cells or to transmit the next valid cell.

HEC Computation Module

The HEC computation module computes HEC on first four header bytes, as indicated by the controller using the polynomial as specified in the ATM UNI 3.1 specification.

Scrambler Module

The scrambler module scrambles only payload octets using the polynomial as specified in the ATM UNI 3.1 specification.

Core Modifications

Normally, modifications are not possible by the user since the core is provided in a Xilinx netlist format. CoreEl can perform special modifications for additional charge. However source code is available for additional cost where the customer can make modifications. Contact CoreEl Microsystems for more information.

Pinout

The pinout is not fixed to any specific device I/O. Signal names for the core are provided in the block diagram shown in Figure 1, and described in Table 1.

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
Data_input[7:0]	Input	Input data bus for transferring in 52-byte cells
SOC_Input	Input	Start of cell indication for input cells
Cell_present	Input	Indicates cell is available to be read in; active high.
Clock	Input	Clock of up to 80 MHz compatible with DS3, E3, STS-3c, and STS-12c applications.
Reset_b	Input	Asynchronous Reset; active low.
Clock_enable	Input	Indicates clock cycles during which module is active.
Data_output [7:0]	Output	Output data containing 53-byte cells with proper HEC.
Read_Enable	Output	Indicates that current clock cycle is being used to read in data; active high.
SOC_output	Output	Start of cell indication; active high.
Cell_txed	Output	Indicates completion of a cell transfer; active high.

Verification Methods

This core has been used in larger ASICs and is silicon proven. The FPGA verification was done by back annotating the implementation and simulating in a Model technology V-System environment.

The test bench was written in VHDL and provides fully automated verification.

Recommended Design Experience

Knowledge of ATM technology and ATM Forum specifications is needed. User should be familiar with HDL design methodology including FPGA targeting. Using the testbench requires familiarity with V-System of Model Technology.

Available Support Products

CoreEl offers a test bench for verifying the core along with a complete line of ATM Core Cells for Xilinx FPGAs that perform the following functions:

- UTOPIA Slave Interface
- Cell Delineation
- CRC-32
- CRC-10

Ordering Information

For information on this or other products mentioned in this specification, contact CoreEl Microsystems directly from the information provided on the front page.

Related Information

The ATM Forum

The ATM Forum publishes specifications regarding ATM. For more information, contact them as follows:

ATM Forum
Worldwide Headquarters
2570 West El Camino Real, Suite 304
Mountain View, CA 94040-1313
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Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
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