XC4000 Series Edge-Triggered and Dual-Port RAM Capability

Summary

The XC4000E and XC4000EX FPGA families provide distributed on-chip RAM. Select-RAM™ memory can be configured as level-sensitive or edge-triggered, single-port or dual-port RAM. The edge-triggered capability simplifies system timing and provides better performance for RAM-based designs. The dual-port mode offers new capabilities and simplifies FIFO designs.

Xilinx Family

XC4000E, XC4000L, XC4000EX, XC4000XL

Demonstrates

Clocked or edge-triggered RAM
Dual-port RAM

The XC4000E FPGA family is a pin- and bitstream-compatible superset of the Xilinx XC4000 FPGA family. It provides increased performance, improved capabilities, and new features. The XC4000EX family of very large devices also includes all of the new features offered in the XC4000E.

Some of the more prominent new capabilities involve the distributed on-chip RAM found on XC4000-Series devices. Although XC4000E/EX FPGAs maintain all of the capabilities found on XC4000 devices, new capabilities include:

- Synchronous or edge-triggered RAM writing that simplifies timing and improves performance. Careful timing relationships between Address, Data, and Write-Enable are no longer required.
- Dual-port RAM mode that provides simultaneous read/write capability. This mode is especially useful for building FIFOs and buffer memories. Dual-port RAM is always edge triggered.
- The ability to pre-initialize the contents of RAM on power-up. This simplifies the overall design in that RAM values are automatically defined. No additional logic is required to perform the initialization.

Table 1 describes the relative capabilities of the XC4000 and XC4000E/EX families.

Table 1: RAM Capabilities of XC4000 and XC4000E/EX

Feature	XC4000	XC4000E/EX
On-chip RAM	X	X
Level-sensitive RAM write	X	X
Single-port capability	X	X
Dual-port capability		X
Edge-triggered RAM write		X
Initialized RAM data at power-up		X

Table 2: Storage Capacity for XC4000E/EX RAM Modes

RAM Mode	Capacity/CLB
Single Port	32x1 or 16x2
Dual Port	16x1

The dual-port capability comes at the price of decreased RAM capacity. Due to the way the dual-port RAM is implemented, and because only four address lines are available, dual-port mode has only half the effective storage capacity of single-port mode, as summarized in Table 2.

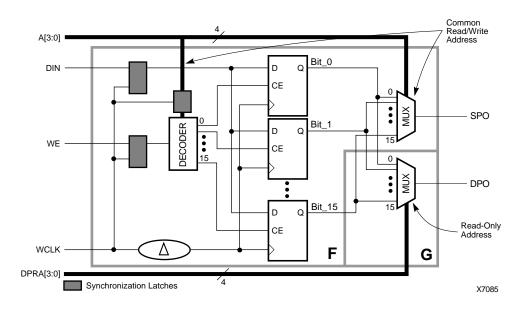## XC4000-Series Conceptual Model

Figure 1 shows a conceptual model of the XC4000-Series RAM. This diagram will be used to describe the various edge-triggered and dual-port capabilities available within each logic block. In this example, the logic block is configured as a 16x1, dual-port, edge-triggered RAM.

This diagram is not intended to convey the actual circuit implementation, but rather to describe the functionality.

Edge-Triggered Write

The XC4000 Series provides both level-sensitive and edge-triggered write capabilities. Both options are available for single-port mode, while dual-port mode is always edge-triggered. Most designers are familiar with level-sensitive RAM. This type of RAM is similar to most SRAM devices available on the market.

One disadvantage of level-sensitive RAM is that it requires a careful timing relationship between the Address, Data and Write-Enable signals. Maintaining such relationships inside an array-based device can be difficult, because the designer does not have direct control over the routing delays within the device.

Figure 1:   XC4000-Series Conceptual Model

However, a better approach for system design is to use synchronous or edge-triggered RAM. Edge-triggered writing simplifies the RAM timing. Instead of a complex relationship between various timing parameters, XC4000-Series RAM timing operates like writing to a data register. Data and Address are presented. The register is enabled. Then a clock edge loads the Data into the register, as shown in Figure 2.

A write operation uses the signals described in Table 3. These signals are derived from Figure 1. The lower right corner of Figure 1—the shaded box labeled 'G'—should be ignored temporarily but is discussed later under "Dual-Port Mode."

During a Write operation, Data is presented on the D input. The write location is presented on the Address inputs, A[3:0]. The RAM block is enabled for writing by a logic High on the write-enable input, WE.

The Write Clock input, WCLK, can be configured as active on either the rising edge (default) or the falling edge. The rising edge will be used throughout these examples. On the rising edge of the Write Clock, the D, A[3:0], and WE inputs are captured, thereby synchronizing them to the clock.

A short delay, indicated by the delta symbol (Δ) in Figure 1, allows the signals to propagate through the decoder logic that enables the appropriate flip-flop. The data is clocked

into the enabled flip-flop by the delayed clock edge. The new RAM data is available on the SPO output a short time later.

The Write Clock input to the logic block is the same input used to clock the CLB flip-flops, although it can be independently inverted. Consequently, the Write Clock input is best driven from one of the global clock buffers (BUFGP or BUFGS for the XC4000E, BUFGLS or BUFGE for the XC4000EX).
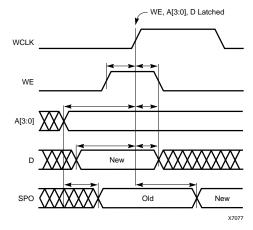

Figure 2:   Edge-Triggered RAM Write Cycle

Table 3: Edge-triggered RAM Description

Signal	I/O	Description
A[3:0]	I	Address input for reading and writing the RAM. The RAM data are available on SPO.
D	I	RAM Data input.
WE	I	Write Enable input. When High, the RAM may be written with the data presented on the D input.
WCLK	I	Write Clock input. Clocks the data into the RAM when WE is High. Also captures and synchronizes the A[3:0], D, and WE inputs.
SPO	O	Single-port output from the RAM. The RAM location is controlled by the A[3:0] inputs. SPO is not controlled by the WCLK input.

Dual-Port Mode

Most RAMs have a single address port and a single output port. These are called single-port RAMs. However, some applications require more than one port. FIFOs are one example of an application that benefits from additional output and address ports.

In a FIFO, there are separate read and write addresses for the memory. A FIFO can be implemented using a single-port memory by multiplexing both the read and write addresses onto a single address port. This approach, however, prevents a simultaneous Read and Write operation. Either a Read or a Write operation can access the RAM at different times, but not both at the same time.

These extra multiplexers and their associated control logic add to the complexity of a RAM-based FIFO design. A dual-port RAM—one with two Address inputs and two outputs—would simplify a FIFO design.

Again, Figure 1 provides an example. The logic in the figure is configured as a 16x1 edge-triggered dual-port RAM. Data can be read and written using the A[3:0] address port and the RAM data appears on the SPO output, just as it would for a single-port RAM.

Simultaneously, data can be read—but not written—using the DPRA[3:0] address port and the RAM data appears on the DPO output. Operations with the DPRA[3:0] address port are independent of the A[3:0] address port. Consequently, a RAM location can be accessed simultaneously through two different locations using the two sets of address and data ports as described in Table 4.

Table 4: Address Port Functionality

Address Port	Operation
A[3:0]	Read and Write
DPRA[3:0]	Read only

If both addresses point to the same location and a Write is performed using the A[3:0] inputs, data appears on SPO and then on DPO a short time later. The DPO output should be used as the primary data output for FIFO designs.

The dual-port mode signals include those shown in Table 3 plus a few additional signals described in Table 5.
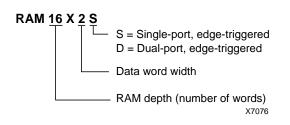
Schematic Symbols

Using the XC4000-Series edge-triggered and dual-port RAM capabilities requires special schematic symbols available within the XC4000E and XC4000EX libraries.
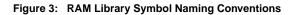
All edge-triggered RAMs have symbols that begin with 'RAM' and end with either 'S' or 'D'. Single-port edge-triggered RAMs end with 'S"; dual-port RAMs end with 'D'. If no letter is appended, the level-sensitive RAM is referenced. All dual-port RAMs are implicitly edge-triggered.

Figure 3 shows an example of RAM library symbol naming conventions.

Table 5: Additional Signals for Dual-Port Mode

Signal	I/O	Description
DPRA[3:0]	I	Dual-Port Read Address (DPRA) input for reading from the RAM. The RAM data are available on DPO.
DPO	O	Output from the RAM. The RAM read location is controlled by the DPRA[3:0] input. DPRA[3:0] is not controlled by the WCLK input.

RAM 16 X 2 S

S = Single-port, edge-triggered
D = Dual-port, edge-triggered

Data word width

RAM depth (number of words)

X7076

Figure 3: RAM Library Symbol Naming Conventions

Initializing RAMs

The contents of an XC4000E RAM can be initialized at power-up. Initial contents are defined by attaching an 'INIT' attribute or property to the RAM symbol, as described in the schematic library guide.

If not defined, all XC4000-Series RAM contents are initialized to all zeros, by default.

NOTE: RAM initialization occurs *only* during configuration. The RAM contents are not affected by Global Reset.

Software Support

The edge-triggered and dual-port capabilities are supported in XACT*step* version 5.2 or later. A software update may be required.

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