3.3 V and Mixed Voltage Compatible Products

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The use of advanced deep-submicron IC fabrication processes is resulting in rapidly increasing density and performance for programmable logic devices, as evidenced by the XC4000XL FPGA family. However, as device geometries shrink below 0.5 microns, the smallest transistors cannot withstand 5 volts without damage. Thus, the largest and fastest new devices are based on lower supply voltages, such as the 3.3 V standard.

To reap the benefits of advanced process technology - including increased performance, increased density, lower power consumption, and lower price - many programmable logic users are making the transition from the 5.0 V standard to lower voltages. This transition affects not only the supply voltage, but also I/O signaling levels. Xilinx is taking an active lead in working with programmable logic users to plan an orderly transition from one voltage standard to the next.

Xilinx introduced the Zero+™ product line, the industry's first 3.3 V FPGAs, in 1993. Since then, the number of 3.3 V product offerings has increased dramatically. For example, the new XC4000XL FPGA family, featuring the industry's highest-capacity high-performance FPGAs, is based on the 3.3 V standard.

However, many other system components remain available in 5.0 V versions only. Thus, mixed-voltage systems (i.e., systems employing a mix of 5.0 V and 3.3 V components) are likely to be the rule rather than the exception in the immediate future. Xilinx products have been designed with this in mind (see Table 1). 5.0 V input tolerance has been designed into many Xilinx 3.3 V devices; these devices accept 5.0 V signals on all I/Os and can drive TTL levels into any 5.0 V device, eliminating any interface issues. Many Xilinx 5.0 V components can directly interface with 3.3 V devices. Future devices will feature multi-voltage I/Os capable of interfacing between a variety of I/O standards.

All Xilinx device inputs maintain their excellent protection against Electro-Static Discharge (ESD), even in mixed-voltage applications.

The following is a brief description of Xilinx devices suitable for use in 3.3 V and mixed 3.3/5.0 V systems. Complete data sheets for the products mentioned below can be found in Chapters 3 and 4 of this Data Book. 3.3 V versions of the Serial PROM devices also are available (see Chapter 6).

FPGAs

3.3 V FPGAs with On-Chip RAM: XC4000XL and Spartan-XL

The XC4000XL family is the broadest and highest-capacity 3.3 V FPGA product line in the industry, with ten devices ranging from 465 to 7,448 logic cells (about 5,000 to 85,000 logic gates). The Spartan Series of high-performance, low-cost FPGAs offers five devices ranging from 238 to 1,862 logic cells. The XC4000XL and Spartan-XL devices meet the specifications of 3.3 V PCI applications. See Chapter 4 for complete product descriptions.

3.3 V FPGAs Without On-Chip RAM: XC3100L

The two members of the XC3100L FPGA family are fast 3.3 V FPGAs. See Chapter 4 for complete product descriptions.

3.3 V Zero+ Family of Ultra-Low Power FPGAs: XC3000L

The XC3000L FPGA devices have quiescent supply currents below 1 mA, with some below 50 µA. See Chapter 4 for complete product descriptions.

5.0 V FPGAs for Mixed-Voltage Systems: XC4000E/EX and Spartan Series

The 5.0 V XC4000E/EX and Spartan FPGA families feature a unique output structure that makes them suitable for mixed-voltage system applications. When configured in TTL mode, the XC4000E/EX and Spartan devices can be directly mixed with 3.3 V devices, as described below. See Chapter 4 for complete product descriptions.

CPLDs

5.0 V CPLDs for Mixed-Voltage Systems: XC9500

Xilinx CPLDs are an excellent fit for mixed-voltage systems. The Input/Output (I/O) ring can be powered by either a 5.0 V V_{CCIO} or a 3.3 V V_{CCIO}. Independent of the V_{CCIO} voltage level, the inputs can accept 5.0 V and 3.3 V inputs. The rail-to-rail output level is defined by V_{CCIO}. These single-chip solutions function extremely well in mixed-voltage systems without any performance penalty. See Chapter 3 for complete product descriptions.

Table 1: Supply Voltage Options

	Device Family	Availability	Accepts 3.3 V Device Outputs[1]	Drives 3.3 V Device Inputs	Key Features
Single Supply V_{CC} = 5.0 V	XC3000A	Now	Yes	With limiting resistor	Low quiescent current
	XC3100A	Now	Yes	With limiting resistor	High performance
	XC4000E/EX	Now	Yes	Yes	Highest density and performance
	Spartan	Now	Yes	Yes	High performance, low cost
	XC5200	Now	Yes	With limiting resistor	Most cost-effective
	XC9500	Now	Yes	With limiting resistor	5.0 V in-system-programmable, pin locking

	Device Family	Availability	Accepts 5.0 V Device Outputs	Drives 5.0 V Device Inputs	Key Features
Single Supply V_{CC} = 3.3 V	XC3000L	Now	With limiting resistor	Yes	Very low powerdown & quiescent current
	XC3100L	Now	With limiting resistor	Yes	High performance
	XC4000XL	Now	Yes	Yes	Highest Density & performance
	Spartan-XL	3Q98	Yes	Yes	Cost-effective, high performance

Dual Supply V_{CC} = 5.0 V V_{CCIO} = 3.3 V	Device Family	Availability	Accepts 5.0 V Device Outputs	Drives 5.0 V Device Inputs	Key Features
	XC9500	Now	Yes	Yes	Mixed-voltage system capable

Notes: 1. Device Inputs must be configured for TTL thresholds.

Interfacing Between 5.0 V and 3.3 V Devices

Today, many designs must accommodate both 3.3 V and 5 V components on the same board. Since both types of supply share a common ground, there are no problems interfacing logic Low levels in either direction, but there are compatibility issues for the logic High levels.

3.3 V Devices Driving Inputs on 5.0 V Devices

The lowest output High voltage (V_{OH}) of the 3.3 V device must exceed the V_{IH} requirements of the 5.0 V device. Minimum V_{OH} for all Xilinx 3.3 V devices is 2.4 V, well above the 2.0 V minimum High level for TTL signaling. (This includes the XC3000L, XC3100L, XC4000XL, and Spartan-XL FPGA families and the XC9500 CPLD family when V_{CCIO} = 3.3V.) Thus, all Xilinx 3.3 V devices can drive inputs to devices with TTL-compatible input thresholds, including all 5.0 V Xilinx devices. (Note: Some Xilinx 5.0 V devices can be programmed for TTL or CMOS input thresholds; these devices must be configured for TTL-compatible inputs to be directly driven from a 3.3 V device.)

5.0 V Devices Driving Inputs on 3.3 V Devices

The highest 5.0 V device output voltage must not force excessive current into the input of the 3.3 V device. The input structures of Xilinx 3.3 V FPGAs include input protection circuits. These protection circuits in the XC3000L and XC3100L devices are designed for 3.3 V inputs. However, the protection circuits in the XC4000XL and Spartan-XL devices are designed to withstand 5.0 V inputs.

Most 5.0 V devices have complementary CMOS outputs where V_{OH} can reach the 5.0 V rail. (All Xilinx 5.0 V FPGAs and CPLDs, except the XC4000E/EX and Spartan series devices in default TTL mode, have complementary CMOS outputs. The XC4000E/EX and Spartan devices can be set to CMOS outputs with the design software.) When driving XC3000L and XC3100L inputs (and most other 3.3 V devices) from such a 5.0 V device, the input current must be limited by a series resistor of no less than 150Ω. This guarantees an input current below 10 mA, flowing through the ESD input protection diode backwards into the 3.3 V supply. That amount of input current is generally considered safe, causing neither metal migration nor latch-up problems. Care must be taken to avoid forcing the nominally 3.3 V supply voltage above its 3.6 V maximum whenever a large number of active High inputs drive the 3.3 V device, potentially causing the 3.3 V supply current to reverse direction. The 3.3 V V_{CC} power should be on before driving the device inputs from a 5.0 V device.

The I/O structures of the XC4000XL and Spartan-XL FPGAs have been designed to tolerate being driven to a 5.0 V rail by a low-impedance source. These 3.3 V FPGAs can be directly driven by 5.0 V devices with either TTL or CMOS outputs. Power supply sequencing is not a problem; the inputs can be driven to 5.0 V either before or after the 3.3 V V_{CC} power is supplied without risking damage to the devices.

In mixed voltage systems, the XC9500 CPLD family can be driven directly by 5.0 V inputs when set up for 3.3 V I/O

operation (i.e., V_{CCIO} = 3.3 V). The input protection circuits in these CPLDs are always connected to the 5.0 V V_{CC} power line, allowing them to tolerate 5.0 V inputs without the need for current-limiting resistors.

If the 5.0 V device has “totem-pole” n-channel-only outputs (as in the default setting of the XC4000E/EX and Spartan FPGA series), V_{OH} is reduced by one threshold and the series resistor can be eliminated, provided the nominally 5.0 V supply does not exceed 5.25 V (as described in detail in the following section). Thus, the XC4000E/EX and Spartan FPGAs can directly drive any 3.3 V device without the need for current-limiting resistors.

Using the XC4000E/EX and Spartan FPGAs in Mixed-Voltage Systems

As a default option, all XC4000E/EX and Spartan devices have a TTL-like input threshold (compatible with 3.3 V output levels) and an n-channel-only “totem-pole” or TTL-like output structure, with an n-channel transistor pulling the output to a V_{OH} level that is one threshold below V_{CC}.

At a nominal 5.0 V V_{CC}, the unloaded output High voltage V_{OH} is less than 3.7 V. When applied to the input of a device with a nominal 3.3 V V_{CC}, there is no additional input current, and the input level does not violate the conventional specification that prohibits input voltages more than 0.5 V above V_{CC}. See Figure 1.

If both 5.0 V and 3.3 V supply voltages track reasonably between their maximum and minimum values, there will never be any additional input current in excess of 1 mA at any commercial or industrial operating temperature.

A worst-case analysis of the interface might assume the (unrealistic) condition where the 5.0 V supply is at its maximum value (5.25 V for commercial applications), while the 3.3 V supply is at its minimum value of 3.0 V. Under these conditions, the interface violates the conventional specification, and drives current into the input of the 3.3 V device, as shown in Figure 2. However, as explained below, this interface is reliable.

For protection against electro-static discharge (ESD), most CMOS inputs and I/O pins usually have a diode between the pin and the nearest V_{CC} connection. This diode prevents the input from going substantially more positive than V_{CC}, which might destroy the input transistor by rupturing its gate oxide. At room temperature, this ESD protection diode conducts negligible current at < 0.6 V forward bias, and conducts ~1 mA at ~0.7 V forward bias, typical for any silicon junction diode. These voltages have a predictable negative temperature coefficient of –2 mV per degree C. At 85 degrees C, these voltages are, therefore, 120 mV lower.

Figure 1 superimposes the output characteristic of the XC4000E/EX and Spartan, and the input current characteristic of a typical 3.3 V device input. Both supply voltages are at their nominal value, but the die temperatures are at their worst-case value of 85 degrees C, and worst-case processing is assumed.

Figure 2 shows the same curves, but with 5.25 V and 3.0 V V_{CC} respectively. The intersection of the two curves defines the worst-case operating point of 3.8 V and 6 mA. That means that the XC4000E/Spartan output drives 6 mA into the forward-biased ESD protection diode, raising the input voltage 0.8 V above 3.0 V, the assumed lowest value of the nominally 3.3 V supply voltage.

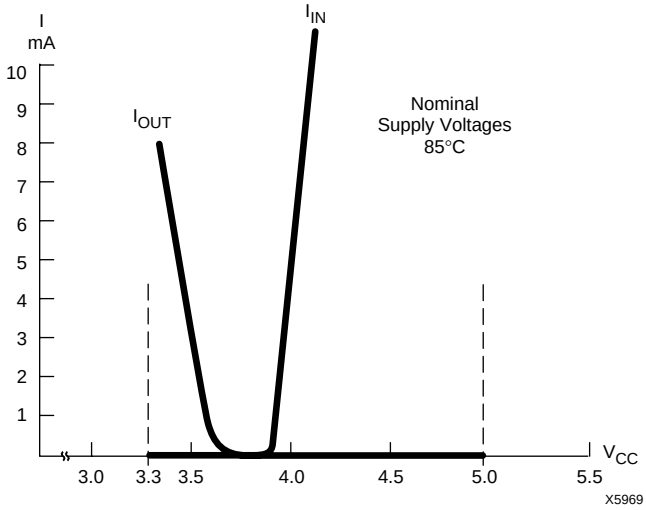

Figure 1: XC4000E/Spartan Output in “TTL-Mode” driving 3.3 V Device Input with Both Supplies at Nominal Voltage (5.0 V and 3.3 V)

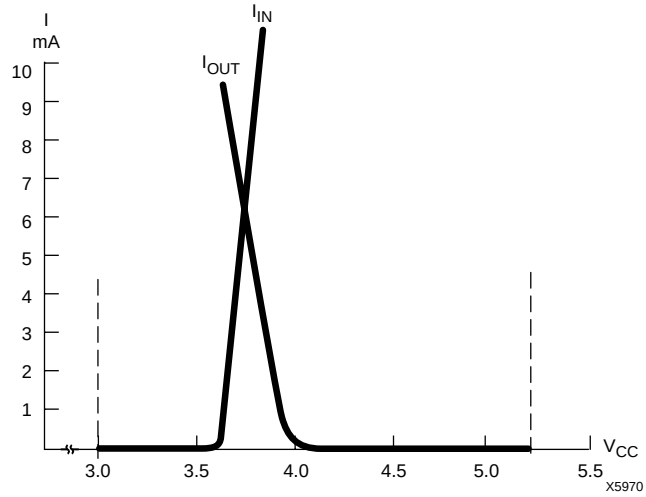

Figure 2: XC4000E/Spartan Output in “TTL-Mode” driving 3.3 V Device Input with Both Supplies at Extreme Values (5.25 V and 3.0 V)

Although this input condition is not covered by the conventional specification, it does not cause any harm and does not affect reliability. ESD protection diodes are designed to conduct hundreds of mA, and the absolute value of the input voltage with respect to ground will never exceed 3.9 V. If the input pin is part of an I/O structure, there is a theoretical possibility of causing latch-up, but all reputable IC manufacturers design their circuits such that latch-up does not occur below 100 mA of input current per pin.

The system designer must estimate the sum of all maximum input currents, and calculate the impact of this current flowing backwards towards the 3.3 V supply. But even if the total 3.3 V supply current goes to zero, V_{CC} for the 3.3 V device is still limited to < 3.6 V (the highest output voltage of the 5 V device minus the forward voltage drop of the ESD diode).

Conclusion

5 V XC4000E/EX and Spartan devices can be freely mixed with 3.3 V devices, without any current or voltage limiting interface resistors, if the following conditions are met:

- The 5.0 V XC4000E/EX and Spartan devices are in their default “TTL mode” with respect to input thresholds and output levels.
- The upper limit on the 5 V V_{CC} is 5.25 V and the lower limit on the 3.3 V supply is 3.0 V, as per standard commercial specifications.
- For industrial operating conditions with higher V_{CC} max, the user must make sure that the absolute difference between the two supply voltages does not exceed 2.20 V. Specifically, if the nominally 5 V V_{CC} is at its max value of 5.50 V, the nominally 3.3 V V_{CC} must not be lower than 3.30 V.