Implementing Median Filters in XC4000E FPGAs

by JOHN L. SMITH,
Univision Technologies Inc.,
Billerica, MA

The median filter is a popular image processing technique for removing salt and pepper ("shot") noise from images. With this technique, the eight direct neighbors and center point of a sliding 3-by-3 array are examined. The median value of the nine elements replaces the original center pixel. The median of the 3-by-3 array is the fifth element in the sorted list of nine elements; thus, the algorithm requires a high-speed sort of the nine pixel values.

The graph of **Figure 1** shows the minimum exchange network required to produce a median from nine input pixels by performing a partial sort. Each node is a two element sort, with the lower input exiting the node on the left, the higher input leaving on the right. The triangular groups of nodes perform a full sort on three elements.

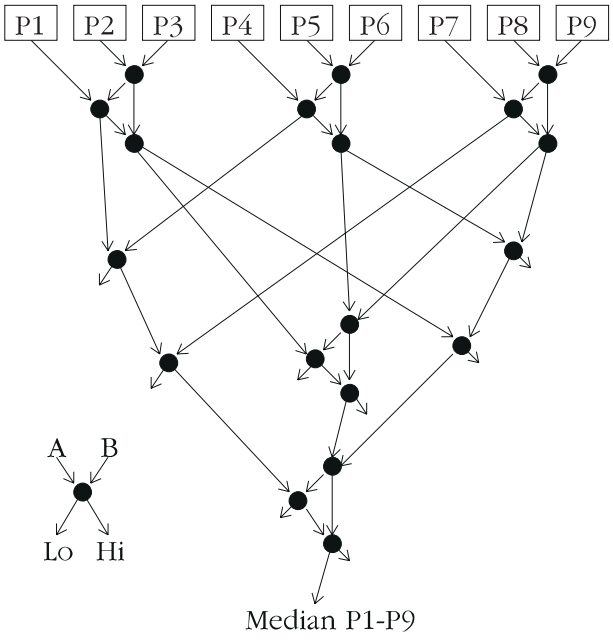

Figure 1: Minimum exchange network required to produce a median from nine input pixels by performing a partial sort

The high-speed carry logic of the XC4000E FPGA is used to implement an efficient compare/swap function. The carry logic in each CLB is set up for an A-B subtract function, while the function generators are used to implement a 2:1 multiplexer. The multiplexer is controlled by the carry out of the subtraction (**Figure 2**). Nodes where both outputs are used may be implemented in nine CLBs (eight for the mux, 1/2 for carry chain initialization, and 1/2 for carry out test); nodes where one output is discarded require only five CLBs.

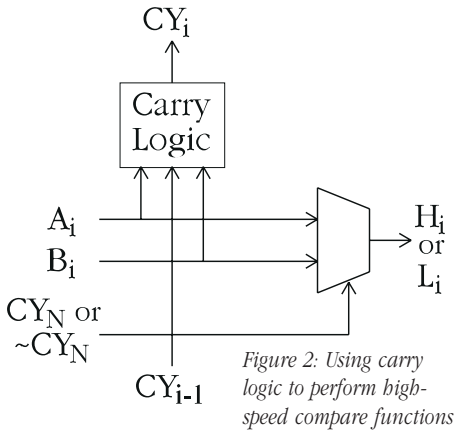

Figure 2: Using carry logic to perform high-speed compare functions

When the circuit is implemented, pipelining can be used so that only three pixels are clocked in at once, eliminating two of the three full sort node groups at the top of the graph (**Figure 3**). In a system with eight-bit pixels, total CLB usage for this real-time median sort circuit is 85 CLBs. ◆

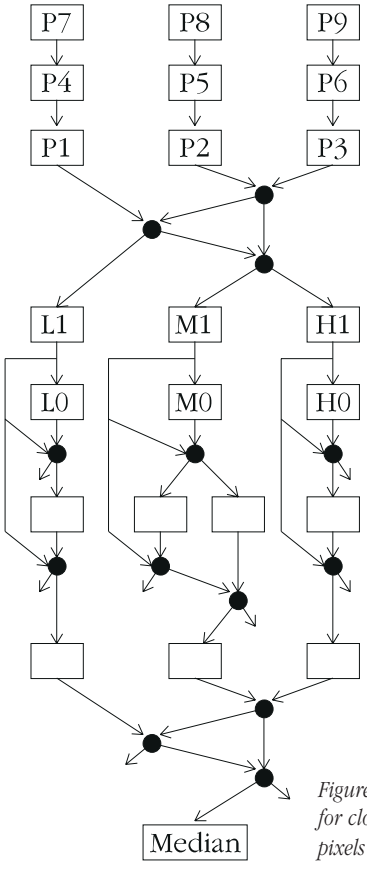

Figure 3: Pipeline for clocking in three pixels at a time

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