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Designing CPLD Multi-voltage Systems

Summary

This application note discusses XC9500XL use in multi-voltage systems.

Introduction

Today's digital systems combine a myriad of chips with different voltage configurations. Designers must interface 2.5V processors with 3.3V memories—both RAM and ROM—as well as 5V buses and multiple peripheral chips. Each chip has specific power supply needs. CPLDs are ideal for handling the multi-voltage interfacing, but do require forethought to ensure correct operation.

Low dropout (LDO) voltage regulators are very useful to create multiple voltages derived from a single master source. Interactions between the "LDO" regulators and the various chips they serve can create frustrating interactions among the chips on a single board. Many designers know these interactions, but are unprepared to deal with power sequences that must be maintained for proper operation of the devices. We will explain the Xilinx XC9500XL family CPLD power characteristics in fairly common system operation. Later, guidelines will be given to systematize designing with these parts.

A Look at XC9500XL Power-up

Many people are unaware that most CPLDs—including the Xilinx XC9500/XL family as well as others—combine both SRAM technology and a nonvolatile technology. Because these CPLDs use sense amp technology, they draw current, even when static. To minimize the current, chip designers transfer internal EPROM bits (E^2 or Flash) to internal latches called "configuration bits." After the bits transfer, the EPROM bits are powered down. This industry standard approach is very effective. It does, however, introduce a "bootstrapping" time for the CPLD during power up.

Figure 1 shows a block diagram of the internal configuration controller, which transfers the EPROM bits to the latches. Some important things to note are:

- The V_{CCint} is sensed to determine when to begin the loading.
- An internal clock source drives a state machine that controls the overall process.
- The bit loading process takes about 100 microseconds.
- There is a small amount of hysteresis on the sensing so that minor V_{CCint} noise will not constantly retrigger the configuration process.
- The state machines, counters and strobes are built from ordinary transistors, so they need setup time, hold time, and propagation delay time to work properly.

The configuration controller is frequently called a Power On Reset (POR) controller. When V_{CCint} passes a threshold, it automatically enables. The state machine cycles through addresses, delivers load strobes to internal latches and completes the process by enabling the I/O pins.

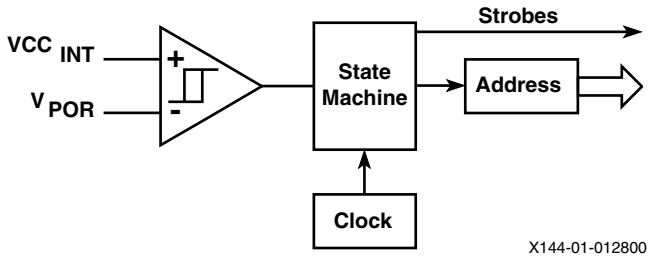

Figure 1: **POR controller**

Figure 2 describes what happens inside the chip as the supply rises to its final value. At low voltage, the transistors do not behave like transistors. As V_{CC} passes about a volt, the transistors begin to wake up, but are not yet fully functional. Above 1 volt, they can amplify and form basic gates. Near 2 volts, they work correctly and can make reliable latches. Above 2 volts, they can be reliably loaded with EPROM bits. It is in this voltage neighborhood the POR circuits begin transferring EPROM bits to the latches.

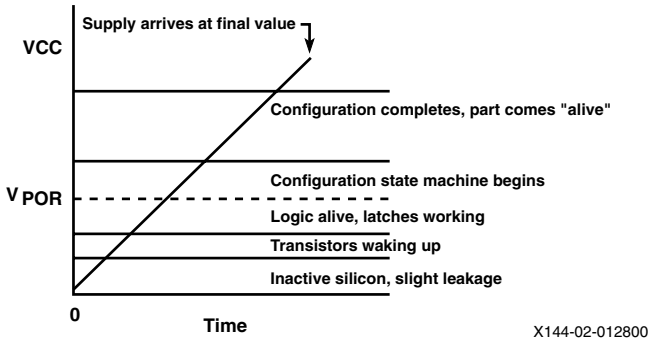

Figure 2: **Power-up activity**

All this activity occurs assuming that the V_{CCint} rises in a straightforward way. If V_{CCint} is noisy or sags below the configuration voltage, the POR circuitry starts over. This restart policy helps because V_{CCint} might drop to a level where the latched bits fail. The result would be improper configuration and unreliable CPLD operation. Restarting is the best policy. However, most systems have some degree of noise on their power supplies, so rather than continuously restart, a small amount of hysteresis in the POR threshold detector makes it robust. This hysteresis is shown in Figure 3 as a ΔV below the POR voltage.

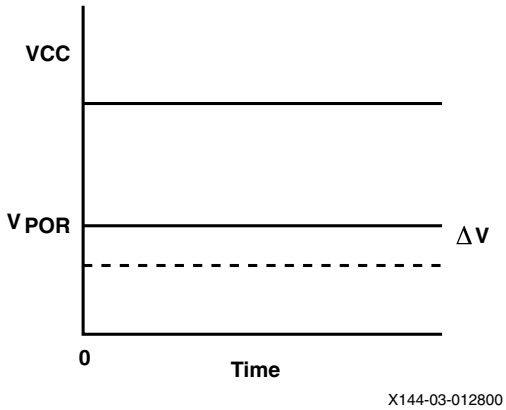

Figure 3: **Relative voltage levels**

A Look at Several Power Supply Scenarios

Figure 4 shows an ideal V_{CCint} rising situation. In theory, if noise-free V_{CCint} rises within a few hundred microseconds, all goes well. V_{CCint} cleanly rises through the POR threshold, configuration load begins, and completes as V_{CCint} reaches the final value. This method always works.

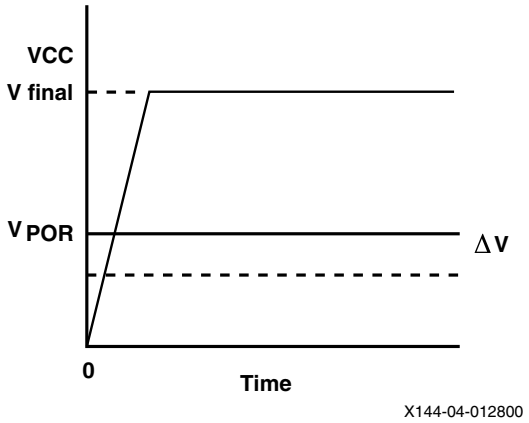

Figure 4: **Ideal V_{CC} rise situation**

Unfortunately, many systems don't have this behavior. Figure 5 shows a slow-rising V_{CCint}. In this case, as long as the voltage is strictly monotonic, all is well. However, noise exists in all systems, making them non-monotonic. Adding a small amount of noise to a slow-rising V_{CCint} can take the POR controller into and out of its configuration process an indefinite number of times. Remember that the controller is made from ordinary flip-flops and gates, so repeated random triggering of the controller can create undefined behavior. This can be externally managed with good power supply design and elimination of noise.

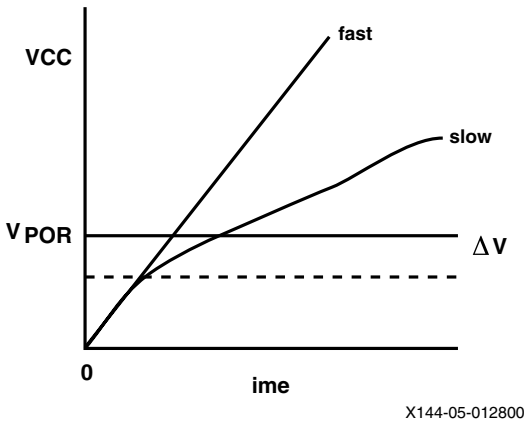

Figure 5: **Slow-rising V_{CC}**

Figures 6 and 7 show additional V_{CC} power-up behaviors occasionally encountered. Figure 6 shows a staged voltage sequence that some systems require. Figure 7 shows a non-monotonic operation of the V_{CCint}, which should be avoided. Either Figure 6 or 7 can be substantially aggravated by the addition of noise, which makes them behave similar to that of Figure 5. The worst case combination of these issues is shown in Figure 8.

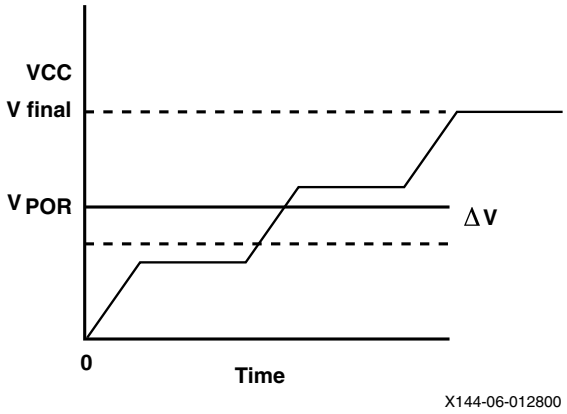

Figure 6: **Staged V_{CC} time**

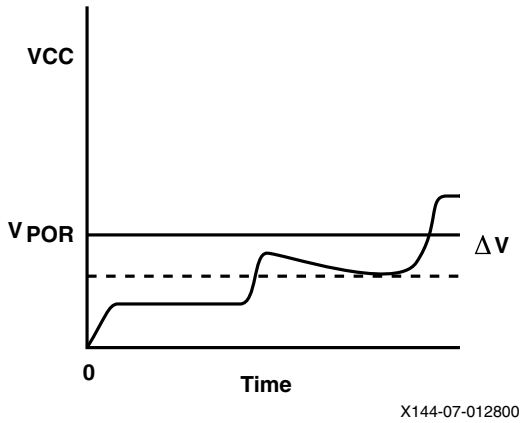

Figure 7: **Non-monotonic V_{CC}**

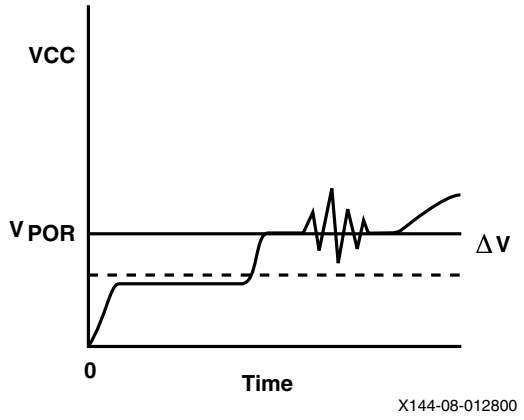

Figure 8: **Noise on top of V_{CC}**

Designing the Power Supply

As we saw, noise can create problems resulting in improper CPLD behavior. Frequently, it is hard to know whether noise is the problem; but when a supply delivers a slow, lagging rise through the POR region and improper configuration occurs, the reason is noise.

One aspect of noise is low current availability. Make certain your supply has enough current to maintain voltage. Decoupling helps, but frequently, a low current LDO regulator is the real problem. Make sure that your LDO regulator has plenty of available current. Do not take the steady state current from the CPLD data sheet as your current target for the power supply; it will be too low. Choose an LDO regulator that has at least one pin-compatible, higher-current version than your target choice. Power-on transients are common among chips, and starving their supply needs is inappropriate.

Designing the CPLD

As mentioned above, ensuring sufficient current is vital for proper power supply operation. You can also help by minimizing the current drawn by your CPLD. First, put as many macrocells as possible into low power configuration. Second, use global resources to reduce the power used by product term resources. Third, use local or pin feedback within the function blocks to lower the total contribution from internal sense amplifiers. Fourth, make sure unused pins are either terminated or connected to user-programmable grounds.

These factors contribute to the total CPLD current usage and can substantially reduce the budget requirements. In all cases, they are simple software options. Naturally, it is assumed that all V_{CC} pins are appropriately decoupled.

Conclusion

Proper power-up sequencing is critical for correct CPLD configuration. Understanding potential pitfalls permits corrective action before problems occur. By taking fairly standard precautions, successful operation of XC9500XL CPLDs can be assured.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
01/31/00	1.0	Initial release.
02/02/00	1.1	Changes title only.