Spartan Series Takes the Lead *with Low Power*

by KIM GOLDBLATT ◆ Applications Engineer

> *"The newest improvements in process technology reduce the power required by Spartan devices even further."*

The new Spartan Series, consisting of the 5-V Spartan and 3.3-V Spartan-XL families, offers an exceptional combination of high performance and low power consumption. Benefiting from an architecture based on segmented routing, Xilinx FPGAs have long dominated the field with an indisputable low-power advantage. The newest improvements in process technology reduce the power required by Spartan devices even further. These advancements together with 3.3-V operation will make the Spartan-XL family the low-power leader in the FPGA industry.

The low-power advantage of the Spartan Series comes at a critical time, when today's large, high-performance FPGA designs are using more power than ever before. As the power goes up, the junction temperature increases proportionally. The thermal equation that governs this relationship is:

$$T_J = T_A + P \bullet \Theta_{JA}$$

where

T_J = Junction temperature

Θ_{JA} = Thermal resistance of the package with die

P = Power dissipation

Keeping control over T_J is important because as it increases, device reliability suffers and delays increase. T_J must not exceed the maximum allowable limit for the package in use, and the maximum T_J for the plastic packages used by the Spartan Series is 125°C.

For more information on thermal relationships, see the article entitled "Power, Package and Performance" from *XCell* #22, pp. 28-29 (you can find it on WebLINX, our web site, at www.xilinx.com/xcell/xcell.htm).

Consideration of the thermal equation leads to a fundamental trade-off: For most FPGAs, the density and performance of a design need to be balanced against the cost of keeping T_J under control. FPGAs without segmented routing commonly require heat sinks and fans to keep T_J within limits. Under normal operating conditions, such measures are not necessary for Spartan devices, which, like all other Xilinx FPGAs, are based on a segmented routing architecture that permits dense, high-performance designs virtually unfettered by power concerns.

As an illustration of the power-performance trade-off, the graph shown in **Figure 1** plots dynamic power (watts) vs. clock frequency (MHz) for two devices of comparable density: the Xilinx XCS30 and the Altera 10K20. Both of these devices are available in the PQ208 package, which has a maximum power limit of 2.28 watts. Beyond this limit, T_J goes above 125°C and a heat sink or fan becomes necessary to avoid compromising device reliability. Note that the Spartan device requires no cooling over its entire operating frequency range (as high as 100 MHz for this counter-based design). For the same design, Altera's 10K20 requires additional cooling when running at 40 MHz or higher.

In today's design environment, with ever more critical power budgeting, you need to select the FPGA family that, by virtue of its architecture and process technology, affords the lowest possible power dissipation. By doing so, you will achieve dense, high-performance designs using fewer parts and less board space. This adds value while cutting costs, resulting in a more competitive end-product.

Comparing FPGA Families

Comparing today's FPGA families for low power requires an objective measure that can show the degree to which device architecture and process technology influence power efficiency. This measure should be independent of design particulars (such as design size and

operating frequency), and be able to isolate the effects of different FPGA families on the overall power dissipation of designs. For reasons explained below, a measure known as "K factor" is well suited to the comparison.

Estimating the power of an FPGA design is not a simple matter. A number of factors contribute to power dissipation, including the clock switching frequency, the design density, the interconnect structure, the number of interconnects switching, and the supply voltage. No one factor tells the whole story. At best, they can be used collectively as a guideline for calculating the power budget. Along these lines, an equation can be used to model the effect of the factors upon Icc as follows:

$$Icc = K \cdot f \cdot N \cdot S$$

where

Icc = Active Icc in µA

f = Clock switching frequency in MHz

N = Number of interconnect lines (logic elements) in use

S = Percent of interconnect lines toggling at any given point in time

K = Icc scale factor

Here, Icc is shown as being directly proportional to the clock switching frequency (f) and the number of signals switching at any given time (N•S). K serves as a constant of proportionality.

To determine the value of K, first fill the FPGA with as many 16-bit counters as possible and use a common clock for all counters. N is 16 times the number of counters that fit into the chip. For 16-bit counters, S is approximately 12.5%, because on average two of the 16 flip-flops in each counter toggle each clock cycle. With this design, Icc is measured across the operating frequency range of the device. The average value for Icc/f together with values for N and S can be substituted into the equation to calculate K.

The K factor can be used to indicate how efficiently different FPGA families use power, because it reflects the influence of device architecture and process technology on the supply current drawn. The K factors for major

Table 1.

K factors for Xilinx and Altera FPGAs Compared

	Xilinx		Altera	
Power Supply	Family	K	Family	K
3.3 volt	Spartan-XL	<28[1]	6KA	55
	XC4000XL	28	10KV, 10KA[2]	29-45
5 volt	Spartan	33	6K	88
	XC4000E	40	10K	82-95
	XC4000EX	47		

1Engineering estimate
2Preliminary information

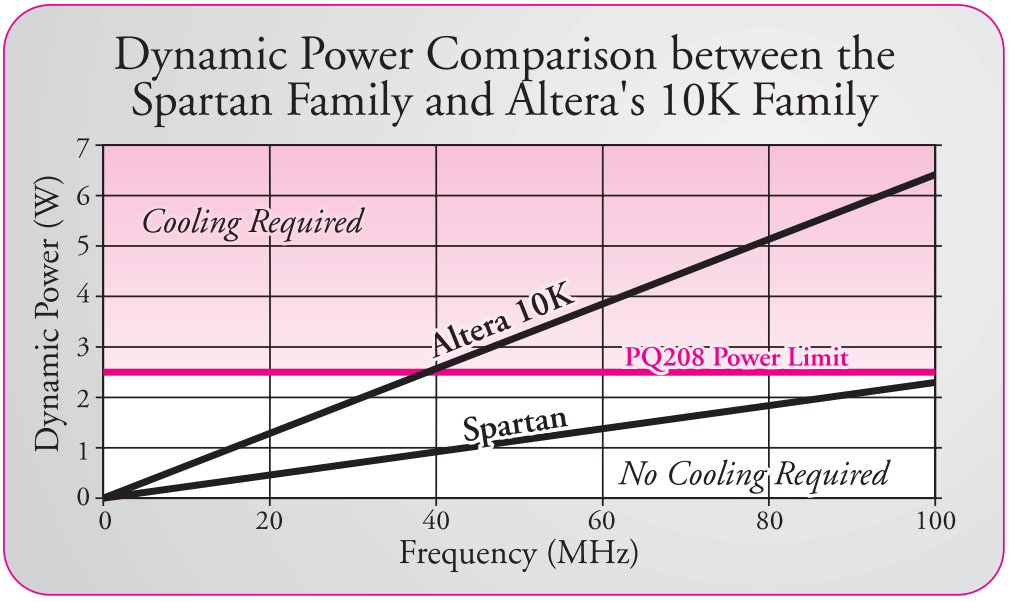

Figure 1.

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Low Power

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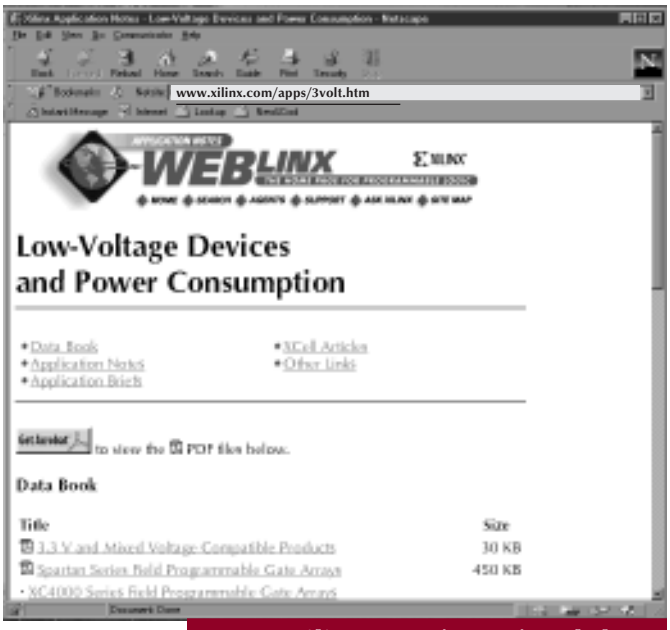
FPGA families from Xilinx and Altera are shown in Table 1. (Altera's data sheets commonly use this model for predicting ICC.)

The K-factors for Xilinx FPGAs are significantly lower than those for similar Altera devices. For example, the Spartan family's K factor (33) is 62% lower than that of Altera's 6K and 10K families (above 82). Thus, for typical designs, the Spartan family uses about 60% less power. As the table shows, for each of the 3.3-V and 5-V operation categories, Xilinx FPGAs exhibit the lowest K values, and thus dissipate less power than their Altera counterparts.



www.xilinx.com/apps/3volt.htm

The Xilinx Low-Power Advantage

The Xilinx low-power leadership can largely be explained by the low capacitance associated with the segmented-routing architecture used on all of our FPGAs. In general, the capacitance of a route is directly proportional to its length. The patented Xilinx architecture uses variable-length routing, which is only as long as needed for a given connection between Configurable Logic Blocks and Input-Output Blocks. As a result, Xilinx FPGAs use significantly shorter routing on average than Altera's FPGAs, which rely heavily on fixed-length long lines. This means Xilinx designs have lower overall capacitance, and thus use less power. The higher levels of power associated with competing FPGAs frequently require not only ceramic packages but also heat sinks and fans.

> *"The most striking observation is that the K-factors for Xilinx FPGAs are significantly lower than those for similar Altera devices."*

Our state-of-the-art process technology makes it possible to reduce power still further. This can be seen in the table, where the Spartan family's K factor of 33 marks an improvement upon the older 4000E family's already low value of 40, resulting in a 17.5% reduction in power.

Finally, 3.3-V operation offers additional power savings over 5-V operation. These savings result not only from the lower supply voltage, but also from the accompanying reduction in ICC. For a 3.3-V supply, ICC and its associated K factor decrease to about 3.3/5 of the value for a 5-V supply. With all else being equal, a 3.3-V Spartan-XL device will use 56% less power than a 5-V Spartan device of comparable density.

Summary

By virtue of segmented routing, an advanced process, and 3.3-V operation, the Spartan Series makes the task of meeting the power budget easier than ever before. As demonstrated by K factor analysis, the Xilinx Spartan Series uses power more efficiently than competing FPGAs, permitting denser, higher-performance designs. For more information on K factor analysis and power in general, consult the "Low-voltage Devices and Power Consumption" section on WebLINX at www.xilinx.com/apps/3volt.htm. Look for application brief XBRF002, entitled "Low-Power Benefits of Spartan and XC4000E/X: An Overview". ◆