APPLICATION NOTE

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XAPP 308

ISP design considerations for CoolRunner™ CPLDs

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ISP DESIGN CONSIDERATIONS FOR COOLRUNNER™ CPLDS

With the introduction of the Coolrunner PZ5128 and PZ3128 CPLDs, Philips Semiconductors entered the realm of ISP, (In System Programming). Now with 32, 64, and 960 macrocell devices, Philips covers the spectrum of CPLDs incorporating ISP. This application note addresses board design considerations, i.e., signal integrity, power supply decoupling, power supply filtering, and component placement that will allow you to utilize the advantages of Coolrunner ISP, in an actual design environment, without headaches.

SIGNAL INTEGRITY

As with any high speed CMOS device, the Coolrunner ISP CPLDs are susceptible to noise as input signals transition from low to high or high to low. This is because CMOS transistors are voltage controlled devices and their input impedances are **VERY** high, typically 10^{15} Ω or more. Therefore even small voltages coupled to the true input signal, during the time when the input has driven the output into its linear region, may cause the output to oscillate, spike, or otherwise behave erratically. This may also induce feelings of unease on your part. Especially if you didn't think about this until AFTER the PCB was laid out. The ISP buffers have protection for this problem in the form of hysteresis and spike rejection; however, no amount of internal device protection can make up for less than adequate board design. If you plan to utilize the ISP capability, it is important to consider the effects of noise pickup and crosstalk. Noise may be introduced into your ISP lines in two main ways:

- Sources external to your board
- Sources on your board

EXTERNAL SOURCES

If you choose to program your Coolrunner ISP CPLD via a download cable, pay close attention to it's construction, (or better still, purchase one from us). The lab, or cubicle, where you work typically contains many sources of radiated electromagnetic energy (read noise). Fluorescent lighting, clock radios, power supplies, test equipment, coffee makers, your computer, etc. can all contribute to a less than benign external environment. Figure 1 illustrates two methods of download cable construction we refer to as 'bad'. As you can see in Figure 1A we have actually built a reasonably good antenna for the reception of unwanted noise. If you build a cable like this you may have problems. The cable design depicted in Figure 1B is a adequate design for the attenuation of external noise. The problem with this cable, however, is crosstalk. We performed extensive testing on a cable constructed as shown in Figure 1B and discovered that significant amounts of energy could be coupled across individual conductors when they ran parallel to one another. Fast edge rates coupled with sufficient drive capability produced enough energy to induce false clocking in adjacent conductors. The amount of energy coupled could be influenced by the orientation of the cable! Clearly not something you would want to rely upon when trying to download new hardware in the field.

Figure 2 depicts a 'good' cable design that has proven itself to be reliable over a wide range of voltage and noise conditions, including many different types and makes of computers.

In this cable the signal conductors are separated from each other by interleaved ground conductors. This arrangement maintains reasonably uniform capacitance throughout the cable length and, to some degree, represents an equivalence to the classical wire over ground transmission line. This combination produces a cable with excellent noise attenuation and crosstalk rejection. The 100 Ω resistors in series with the signal conductors, (located at the computer DB25 connector) serve two purposes. The first is voltage decoupling, the second is series damping. It is unlikely that the output high voltage present on a computer's parallel port data lines and V_{CC} for the ISP CPLD will be the same value. This is especially true when programming 3 volt parts from a 5 volt computer interface. In this situation, the series resistor acts as a voltage decoupler, preventing potentially damaging current from flowing through the device's input protection diode. Series damping is an arcane method of terminating a transmission line. In this form, a series resistor plus the output impedance of the source combine to match the characteristic impedance of the transmission line. For the Philips download cable, 100 Ohms represents a good compromise between output impedance, cable impedance, and standard resistor values. With the series resistor located as close as possible to the signal source it is possible to reduce the source reflection coefficient to practically zero. This absorbs the wave reflection coming back from the load thus terminating the reflection cycle.

The advantages of this type of termination scheme are:

- Very little power is consumed. This is especially important in low power applications, those for which the Coolrunner is perfect.
- Requires only one resistor per signal line.

The disadvantage of this technique is that for a time, (2tpd) the voltage present along the line is $0.5V_{OUT}$. This is not a problem in this application, however, since the signal connections are at the end of the line.

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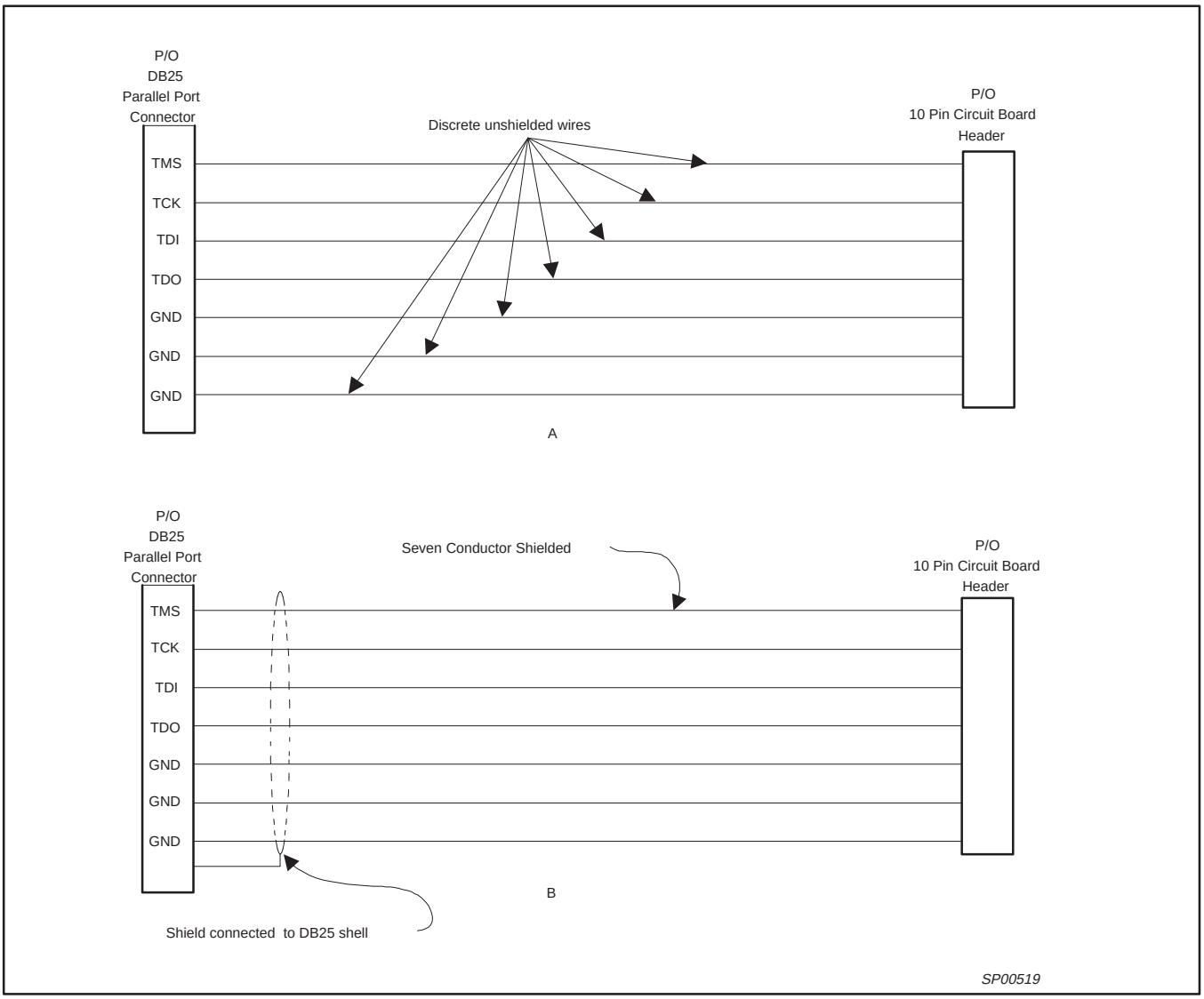

Figure 1. 'Bad' download cable design

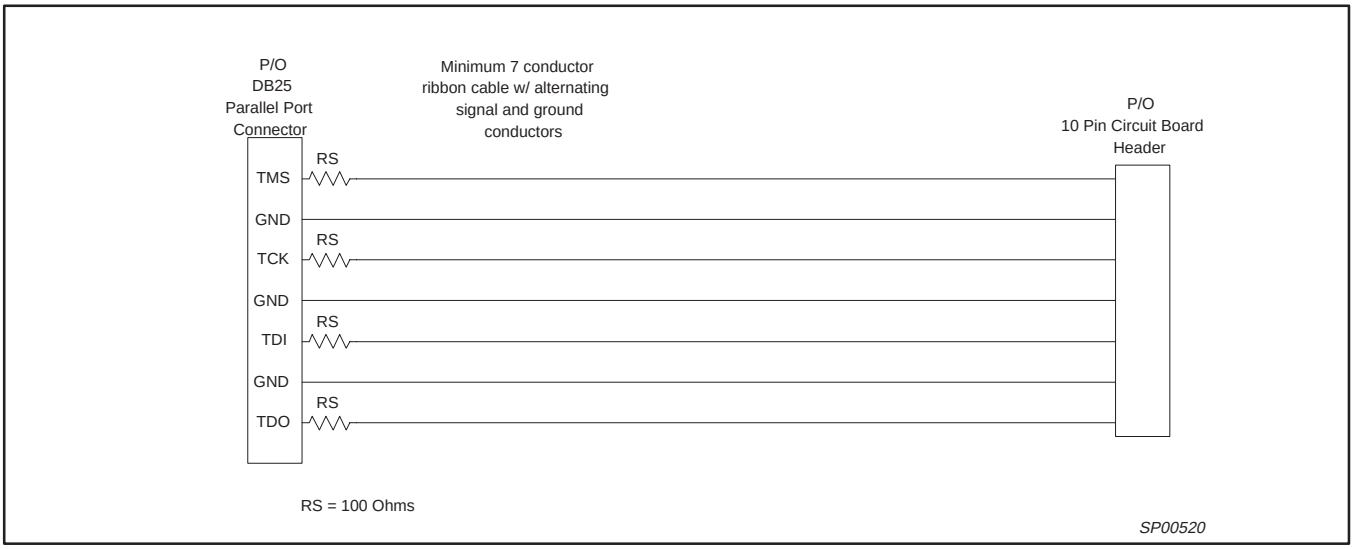

Figure 2. 'Good' download cable design

ON BOARD SOURCES

High performance devices that populate most circuit boards today routinely produce output edge rates of 2 to 4 ns. If the trace length, from device to device, is long enough, transmission line effects must be taken into account. One can calculate when to start worrying by using the formula:

$$L = \frac{t_r}{2t_{pd}} \times \frac{1}{\sqrt{1 + \frac{C_D Z_O}{t_r}}}$$

Where:

- L = trace length
- t_r = rise time
- t_{pd} = calculated propagation delay
- C_D = trace capacitance
- Z_O = calculated characteristic impedance of the trace

Table 1 was generated using this formula. A line propagation delay of approximately 2.3 ns per foot is assumed for the above calculation. This is a typical delay for well constructed printed circuit boards.

Table 1. When to worry about reflections

t_r in nanoseconds	C_D in picofarads	L x 12 to convert to inches
4	10	9.99
4	20	9.46
4	40	8.63
4	80	7.47
2	10	4.73
2	20	4.32
2	40	3.74
2	80	3.05

If your PCB trace length for high clock speed signals has met the criteria for transmission lines, you must terminate the lines. The exact methods and procedures for line termination are beyond the scope of this application note. Suffice it to say, reflections can be considered noise and should be eliminated or reduced on all PCB traces, not just the ones used for ISP.

Crosstalk between adjacent PCB traces is also a noise source to watch for. Try not to run signal lines parallel to one another or, if you must, interleave the signal traces with ground traces. Insure that adequate copper exists to prevent, or greatly reduce, L di/dt rises in ground or dips in V_{CC}. It is also a good idea to have only one point on the board from which ground radiates, this will reduce the possibility of generating ground loops. Please do not tie your analog and digital grounds together, except at the one common point mentioned above. If you don't follow this rule, it will not bother your digital circuitry very much, but your beautiful, elegant, analog designs may not appreciate the interference. I left out power and ground planes because I know I don't even have to mention this requirement, right? If you locate your clocked filter, switching power supply, or any other source of high frequency switching transients near the ISP lines without adequate decoupling you may have trouble. We will talk more about decoupling in the next section. When operating at transmission line frequencies, one must take special care when routing signals on the PCB. The high frequencies that are generated by high slew rate rise times love to launch themselves in space when they encounter right angle turns in your PCB traces. The high impedance inputs on your CMOS devices will be only too happy to include this source of noise as part of the original signal. Make smooth, gradual turns with your traces and you will prosper.

POWER SUPPLY DECOUPLING

Every active device on your PCB should be decoupled from the power supply with at least one capacitor placed across the power and ground pins and located as close as possible to the device. If the device has more than one power/ground pair, then a capacitor(s) will be needed for however many it has. As an example, the PZx128 has eight power and ground pairs therefore you should use

a minimum of eight capacitors to decouple this device. A tantalum or aluminum electrolytic capacitor, 10 μF or larger, should also be provided for every 50 or so active devices on the PCB. These capacitors will reduce power supply ripple and, for best results, they should be located near the point at which the power and ground rails enter the PCB. You may be wondering what value of capacitor to use at each active component. The answer depends upon what you are trying to accomplish. Capacitors located across component power and ground pins, depending upon their value, can perform high frequency decoupling or provide a charge reservoir for rapid changes in device current. To calculate a value for a reservoir capacitor, it may be helpful to use the equation:

$$C = i \frac{dt}{dv}$$

Where:

- C = the capacitor value you are valiantly trying to calculate
- i = the total current your device will consume worst case
- dt = lets call this the output slew rate, or rise time
- dv = a reasonable value of allowable voltage droop

Again using the PZx128 as an example, we find that it has a maximum of 96 I/O lines. If we require every output to turn on at the same time and we set the characteristic impedance of each output trace to 50 Ω, the current required will be 96 x (5V/50 Ω) = 9.6 amperes! This can safely be considered WORST CASE! With a 100 mV drop in V_{CC} and a 2 ns rise time, the capacitance required will be:

$$\frac{9.6\ A \times 2\ ns}{100\ mv} = 0.192\ \mu F$$

A 0.1 μF capacitor for every power/ground pair will therefore handle the maximum instantaneous current requirements quite easily.

FILTERING THE POWER SUPPLY

At high frequencies the 0.1 μF capacitor will look like a hippo as far as filtering is concerned. This is because its resonant frequency, (about 100 MHz) is too low to adequately reduce the high frequency harmonics generated in high performance systems. Without going into an in-depth discourse on Fourier transforms of periodic pulses, let's assume that the fundamental frequency relates to period, the first harmonic is a function of pulse width with the same energy as the fundamental, and that the second harmonic is a function of rise time and contains approximately half the energy of the fundamental. The following generic equation can be used to calculate fundamental and harmonic frequencies.

$$F = \frac{1}{\pi \times T_X}$$

Substitute:

- The period of the clock signal for T_X when calculating the fundamental frequency
- The pulse width of the clock signal for T_X when calculating the 1^{st} harmonic
- The rise time of the clock signal for T_X when calculating the 2^{nd} harmonic

For a system operating at 100MHz with a pulse width of 5 ns, the F_0 is 32MHz, F_1 is 64MHz, and F_2 is 159 MHz.

Using the formula for resonance,

$$f = \frac{1}{2\pi\sqrt{LC}}$$

and plugging in the lead inductance of 1.1nH for a 0.001 μF ceramic capacitor, as determined from it's data sheet, we find that it self resonates at approximately 150 MHz. Attaching this capacitor to a PCB in a most careful fashion, will provide adequate high frequency filtering of your design. Place this capacitor in parallel with the 0.1 μF reservoir capacitor, as close as possible to the active device, with as little total lead length as possible. Those who still experience trouble may want to use chip capacitors instead of leaded ones. This greatly reduces the series L and therefore increases the resonant frequency, giving better coverage of the higher frequency harmonics.

COMPONENT PLACEMENT

The placement of components on a PCB can have enormous impact on the noise environment. You may be less than pleased if you have arranged your CoolRunner™ CPLD and the ISP download header in such a fashion as described in Figure 3. Remember to place the download header as close as possible to the device being programmed. If you are programming our ISP devices from an on-board microcontroller, or an edge connector, it is important to follow the rules set forth in the section entitled **On Board Sources** of noise in this app note.

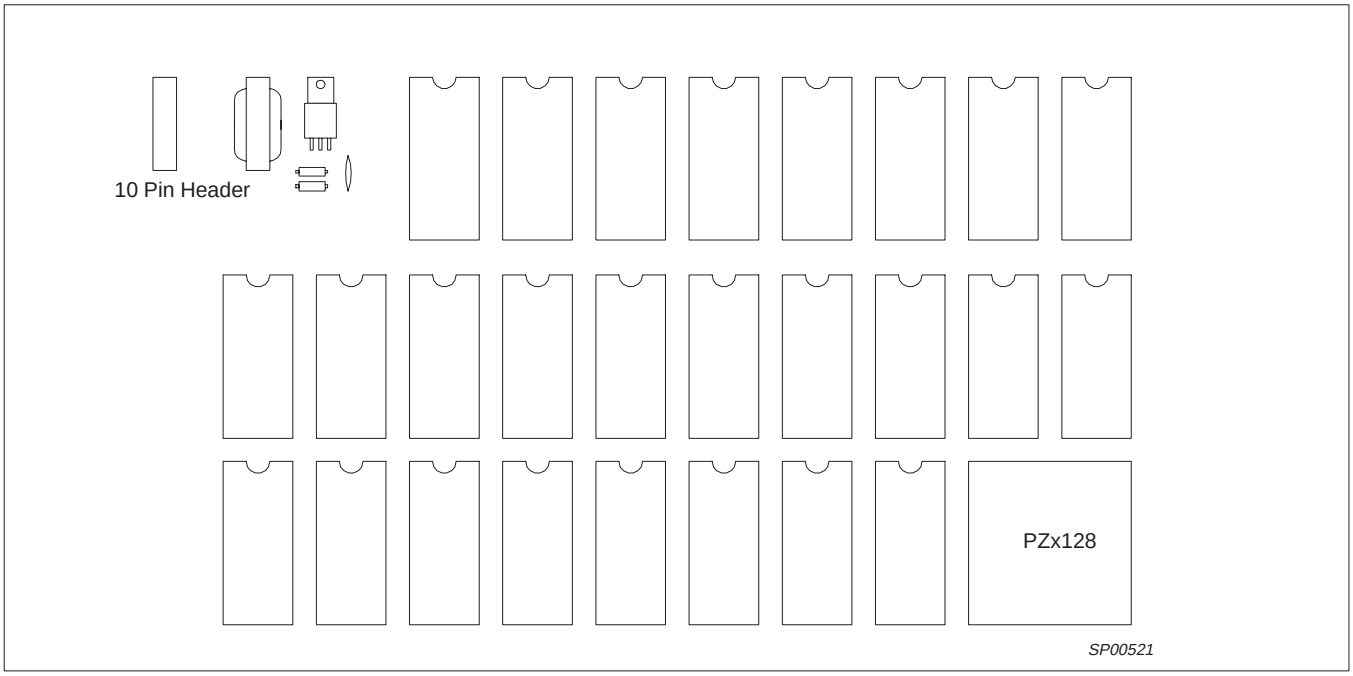

Figure 3. 'Bad' PCB layout

SUMMARY

High performance systems require that close attention by paid to printed circuit board layout, noise sources, and noise coupling. By following a few simple rules it is possible to construct a PCB that will allow you to effectively utilize our ISP devices.

NOTES

ISP design considerations for CoolRunner™ CPLDs AN069

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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