JTAG Boundary-Scan for Low Cost System Testing

Xilinx FPGAs and CPLDs have built-in boundary-scan capability for in-system testing and debugging. This method of incorporating special test circuitry into a device gives you complete control of, and access to, the device pins without the need for external probes. Here's what it's all about.

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Multi-layer circuit boards, using surface mount devices, are extremely difficult to test; that's why the IEEE1149.1 standard, or "boundary-scan" was developed. Boundary-scan is typically used to test the interconnections between devices on a printed circuit board. Each boundary-scan-compatible device allows you to take control of its I/O pins to drive and receive test signals.

Through a simple 4- or 5-wire Test Access Port (TAP), you can shift in a stimulus for all device output pins and then read in the corresponding signals on the receiving devices' input pins. Then you compare the outputs with the inputs to verify the connectivity between devices. This can also help you repair boards by identifying the location of any open or shorted traces. By daisy chaining multiple boundary-scan-compatible devices, you can effectively test a complete circuit board using a single set of test vectors that are input through a single TAP.

Each boundary-scan-compliant device includes a shift register composed of boundary-scan cells, a 4- or 5-wire Test Access Port (TAP), and a state machine (TAP controller), as shown in **Figure 1**. The TAP pins are:

- TCK - This is a clock signal that synchronizes the internal boundary-scan state machine (TAP Controller) operations.
- TMS - This is the internal state machine mode select signal. This signal is sampled at the rising edge of TCK to determine the next state machine state.
- TDI - This is the data input pin. When the internal state machine is in the correct state, this signal is sampled at the rising edge of TCK and shifted into the device's test or programming logic.

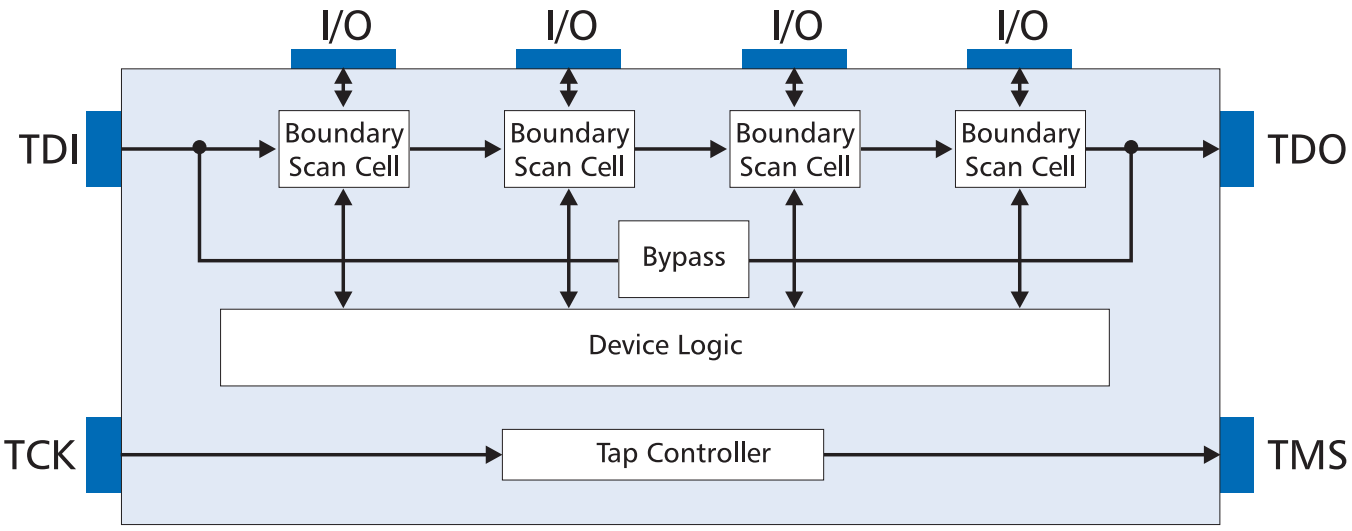

Figure 1

- TDO - This is the data output pin. When the internal state machine is in the correct state, this signal represents the data shifted out of the device's test or programming logic. The output data is valid on the falling edge of TCK.
- TRST (optional) - This is the asynchronous reset pin. When driven low, the internal state machine advances immediately to the reset state. Because the pin is optional and pins are generally high-cost additions to devices, it is usually not implemented. In addition, the internal state machine has a well defined synchronous reset mechanism.

Multiple boundary-scan devices are linked serially in a daisy chain, with all devices sharing the same TCK and TMS signal. The TDO of one device links to the TDI of the next. This results in what appears to be a single shift register of a fixed length from the system TDI pin to the system TDO.

All devices have registers composed of boundary-scan cells, internally linked between the TDI and TDO pins. Under normal operating conditions, these cells are transparent and inactive, allowing signals to pass normally. When the device is placed in the test mode, each boundary-scan cell can either read the state of its associated pin, or drive a signal onto the pin. Thus you can shift in a stimulus vector and shift out the received pattern, in one operation, for all devices in the boundary-scan chain.

Xilinx XC9500 CPLDs also use the TAP pins for device programming. This allows you to both program and test our CPLDs using the same equipment. Plus, this guarantees a reliable programming operation with no danger of lock-up (as seen in some competing devices). XC9500 CPLDs also implement optional boundary-scan instructions that provide additional capabilities (see the XC9500 or XC9500XL data sheets for details).

Conclusion

Boundary-scan is a fast, convenient, and simple method for testing and debugging systems, supported by a wide number of device and test equipment manufacturers.

All Xilinx XC9500 and XC9500XL CPLDs, and all Xilinx FPGAs since the original XC4000 series, include boundary-scan capability.

For More Boundary-Scan Information

For the full IEEE1149.1 standard,
***see**: http://standards.ieee.org/*

A wealth of information on the standard is also available from the Texas Instruments Boundary Scan Page at: http://www.ti.com/sc/docs/jtag/jtaghome.htm.

Serial Vector Format (SVF)

Serial Vector Format (SVF) is the de facto standard for interchange of boundary-scan-based stimulus information. Note that this is not an open standard. It is currently copyrighted and controlled by Asset Intertech but freely distributed.

***See**: http://www.asset-intertech.com/releases/svf.htm*

JEDEC

JEDEC Programming File - more formally known as JESD3-C Standard Data Transfer Format Between Data Preparation System and Programmable Logic Device Programmer.

***See**: http://www.eia.org/eng/allstd/std/files/jedec/jesd3%2Dc.htm*

JEDEC Chain Description File - more formally known as JESD32 Standard for Chain Description File. This file format is meant to describe the connection of arbitrary programmable devices in a serial chain. It is somewhat confused in execution, precariously trying to balance a description of both non-IEEE1149.1 and IEEE1149.1 types of serial chains in the same language. Notably, it is also unable to describe complex boundary-scan chain configurations like hierarchical or multidrop architectures.

***See**: http://www.eia.org/eng/allstd/std/files/jesd32.htm*

BSDL

Boundary-Scan Description Language (BSDL) Standard 1149.lb is used to describe the IEEE1149.1 TAP Controller and boundary-scan register on a boundary-scan-compliant device. BSDL is also implemented as a subset of the VHDL standard.

***See**: http://standards.ieee.org/*