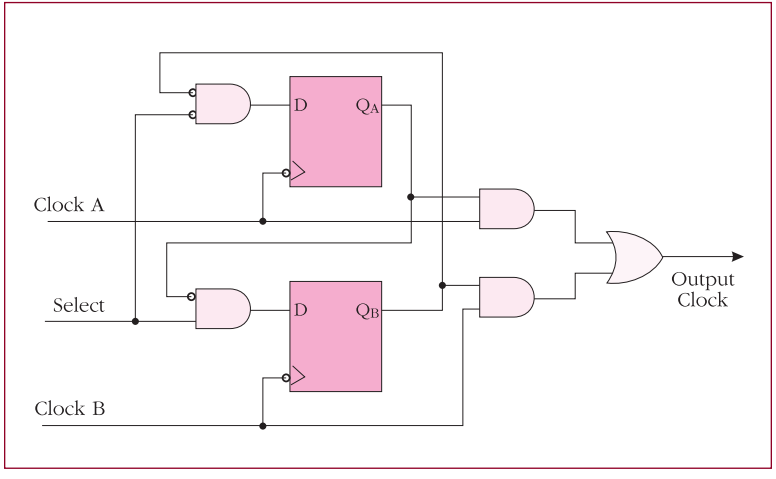
Trouble-Free Switching Between Clocks

Asynchronously selecting between two clock sources can easily produce glitches that cause unreliable system behavior. The circuit diagrammed here avoids these problems.



While the SELECT input is stable (either High or Low), the two control flip-flops are in opposite states and one of the two clock inputs drives the clock output. When the SELECT input changes, there is no immediate impact until after the next falling edge of the originally-selected clock source, which also resets its control flip-flop. The Output Clock signal will then stay Low until the next falling edge of the newly-selected clock. This edge will set its control flip-flop, causing this clock to drive the Output Clock. Thus, with this circuit, any switching between clock sources is delayed by holding the output Low from the time the first clock goes Low until the time the second clock is Low. ◆