One Dimensional Serial ROM-Based Correlator

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Features

- Serial data window selectable from 4 to 128 bits
- Mask parameter allows data bits to be selectively ignored
- Cascadable to form correlator of any length
- Easily extendible to 2 dimensions
- High performance implementation using efficient look-up table design
- Uses Fast Carry logic for high speed
- Drop-in modules for the XC4000E, EX, XL, XV, and Spartan families
- Density and performance guaranteed through Relational Placed Macro (RPM) mapping and placement technology
- Available in Xilinx Core Generator Tool

Functional Description

This module samples the serial data presented on its data-input port (SDIN) on every rising edge that occurs on the clock input (C). The module stores the previous N data samples in internal memory, where N represents the number of bits in the serial data window. The size of the data window, N, is a user selectable parameter (WIDTH) that may vary between 4 and 128 bits, in multiples of 4 bits.

The module takes two additional user parameters, MATCH and MASK, each of which are expressed as N-bit binary values. The correlator's SUM output is a count of the number of bits in the module's internal data memory that match the bit pattern expressed by the MATCH parameter. For example, assuming a data window size of 12-bits, if all 12 bits of stored data match the 12-bit MATCH parameter, the correlator's SUM output returns the value 12. If any of the bits in the module's memory do not match their equivalent bits in the MATCH parameter, the output value is correspondingly smaller.

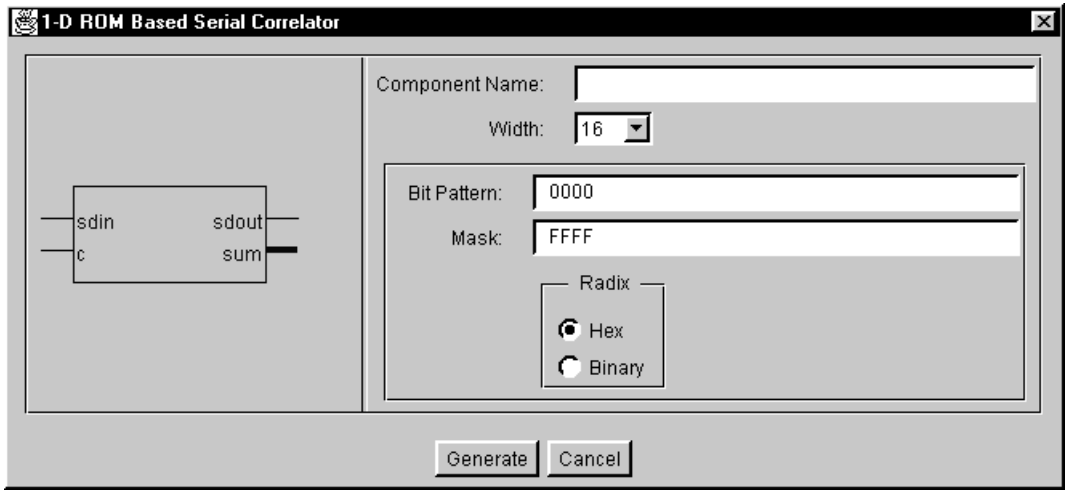

Figure 1: Parameterization Window

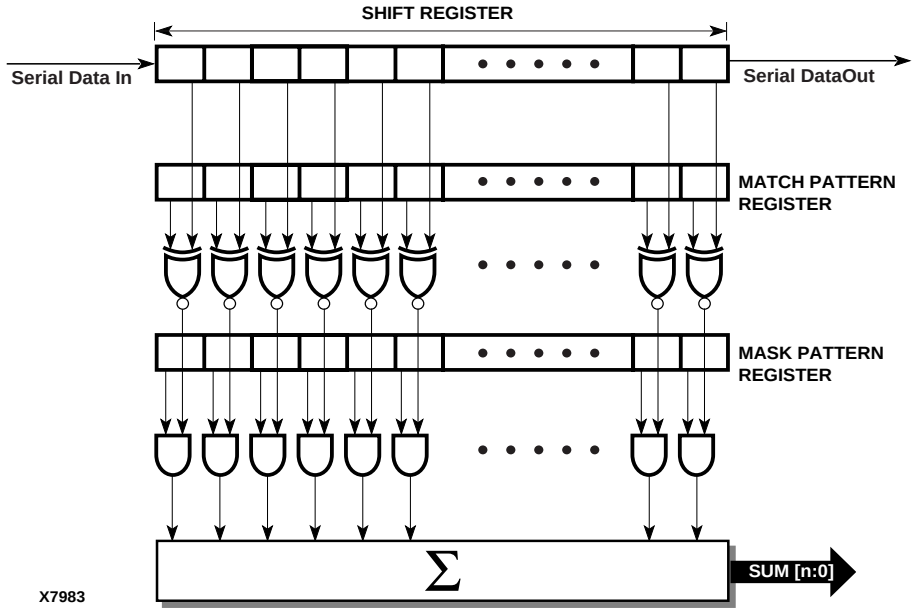

Figure 2: Serial Correlator Functional Block Diagram

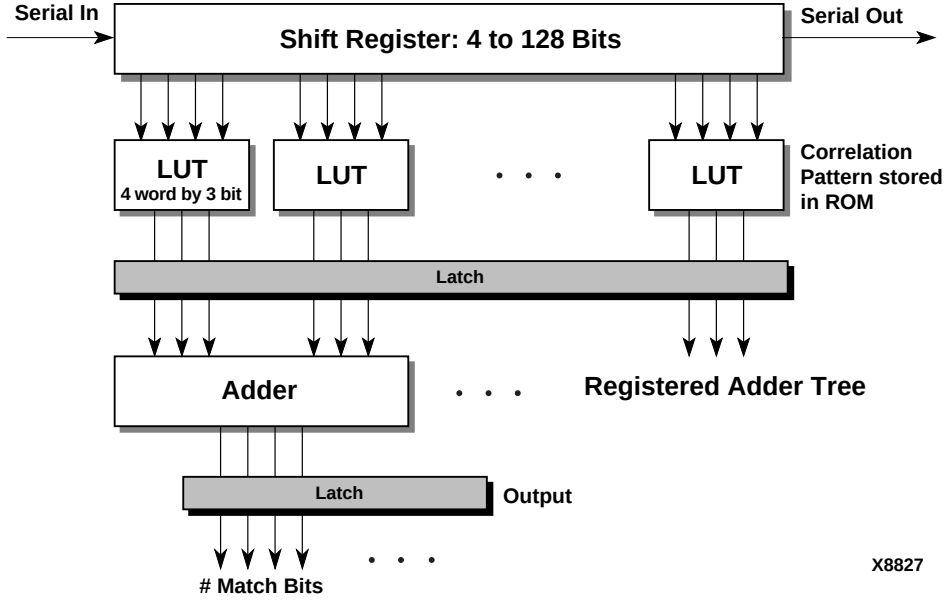

Figure 3: CORE Generator Implementation of Serial Correlator

The MASK parameter allows specific bits in the MATCH parameter to be excluded from the correlation equation. Those bits in the MASK parameter that are set to '1' indicate that the corresponding bits in the input data and the MATCH parameter should be compared, and if found identical, contribute to the correlator's SUM output. Those bits in the MASK parameter that are set to '0' indicate that the corresponding bits in the input data and the MATCH parameter should not be compared, and their match status should not affect the correlator's SUM output. See figures 1 and 2.

The serial data that is stored in the module's internal memory is shifted-out serially on the SDOUT pin and is identical to the data that was presented at the data port (SDIN) N clock-cycles earlier. Correlators may be cascaded, forming larger correlators, by connecting the SDOUT port of one module to the SDIN port of another. The sum of the two correlator's outputs is the result of the combined correlator. (When cascading correlators in this fashion, make each correlator's data window the same size to ensure that the latency through each is identical, and the results from each arrive at their SUM outputs at the same instant.)

This function is often used in data communications to establish synchronization with an incoming serial bitstream, and in any application that requires pattern recognition.

CORE Generator Parameters

The Core Generator parameterization window for this module is shown in Figure 1. The parameters are as follows:

Component Name: Enter a name for the output files generated for this module.

Correlation Width: Select the number of bits in the correlation window. May be any multiple of 4-bits in the range 4 to 128-bits.

Match Pattern: Enter the bit-pattern that the correlator should detect. The pattern may be expressed in hexadecimal or binary.

Mask Pattern: Enter the bit pattern that describes which bits in the Match pattern should be ignored. The pattern may be expressed in hexadecimal or binary. A '0' at any bit-position indicates that the corresponding bit in the match pattern should be ignored.

Radix: Indicate the base used to express the match and mask patterns.

Using Look-Up Tables for Implementing Correlators

The following example illustrates hoe the the CORE Generator calculates the contents of its distributed look-up tables. The example shows a 4-bit correlator with an input match pattern of 1101 and a mask pattern of 1111 (include all bits).

Any N Bit correlator can be decomposed into (n/4) 4-Bit correlators. The LUTs contain all potential outputs for each 4-stage correlation. For example, the correlation pattern 1101 stores 4 at address D in the LUT (all four bits match) and 3 at addresses 5, 9, C, and F in the LUT (three bits match).

Table 1: LUT Contents

Address	Data
0000	001 (1 bit matches)
0001	010 (2 bits match)
0010	000 (0 bits match)
0011	001 (1 bit matches)
0100	010 (2 bits match)
0101	011 (3 bits match)
0110	001 (1 bit matches)
0111	010 (2 bits match)
1000	010 (2 bits match)
1001	011 (3 bits match)
1010	001 (1 bit matches)
1011	010 (2 bits match)
1100	011 (3 bits match)
1101	100 (4 bits match)
1110	010 (2 bits match)
1111	011 (3 bits match)

Combining 4-Input Sections

Each four-input correlator section can be combined by summing the outputs with an adder tree. The look-up tables are 16 words (4 address lines) by 3 bits wide each. The adder tree grows by one bit for each level and the resulting output is a binary number representing the number of matches in the input data word after the mask register has been applied.

Pinout

Pin names for the schematic symbol are shown in Figure 5, and described in Table 2.

The CORE Generator accepts the parameters entered through the dialog box and creates the specific design from the values entered using a parameterized VHDL recipe. VHDL instantiation code and a schematic symbol are created along with the netlist for the design.

Table 2: Core Signal Pinout

Signal	Signal Direction	Description
SDIN	Input	Serial Data In – Serial data input for storage in internal memory.
C	Input	Serial Data Clock – Serial data is captured and new output data is formed on rising clock transitions.
SDOUT	Output	Serial Data Out – SDIN delayed N clock cycles.
$SUM[m:0]_i$	Output	Binary representation of the number of bits that match the correlation MATCH pattern excluding those bits identified in the MASK pattern.

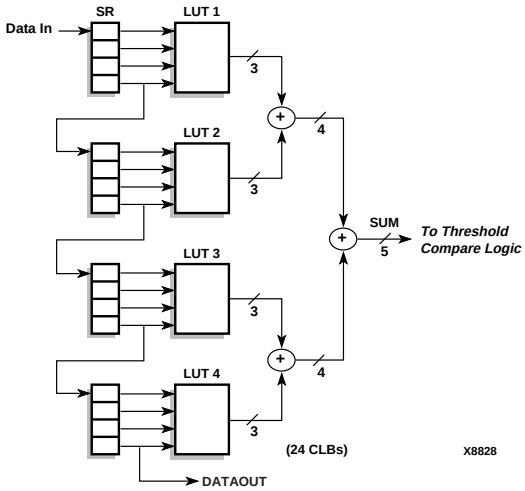

Figure 4: Serial Correlator Schematic Symbol

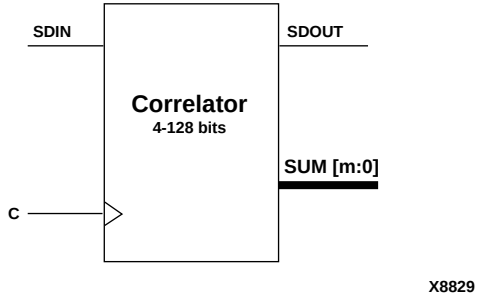

Figure 5: Combining 4-Input Sections

Output Bit Width and Latency

The SUM output bus is M bits wide, where M is sufficient to express the largest value that can be calculated by the correlator. The largest value that the correlator will produce occurs when all bits in the correlation window are identical to all bits in the MATCH parameter and all bits in the MASK parameter are '1's. At this time the correlator's output value will be M, the number of bits in the correlation window. The output bitwidth is therefore $Log_2(M)+1$ rounded down to the previous whole number.

The correlator's latency is a function of the size of the correlation window, N. The function for determining the correlator's latency is as follows:

Table 3: Latency Table

N	Latency
<= 4	1
<= 8	2
<= 16	3
<= 32	4
<= 64	5
> 64	6

Table 4 lists the number of CLBs required for example bit widths. The maximum speed is for XC4000E-1 devices.

Table 4: Bit Width versus CLB Count

Bit Width	CLB Count
4	4
7	11
8	14
9	16
10	17
11	19
12	20
13	22
14	24
15	26
16	25
17	29
20	36
32	54

Ordering Information

This macro comes free with the Xilinx CORE Generator. For additional information contact your local Xilinx sales representative, or e-mail requests to dsp@xilinx.com.

Parameter File Information

Parameter Name	Type	Notes
Component_Name	String	
Mask	Hex/Binary String	
Bit_Pattern	Hex/Binary String	
Width	Interger	4 to 128 multiple of 4