Registered Dual Port RAM

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Features

- Supports data widths from 2 to 31 bits
- Supports memory depths from 16 to 256 words
- Uses SelectRAM™ for high density and performance
- Allows power-on memory contents to be defined.
- Two access ports permit simultaneous read/write operations to separate locations
- Two registered outputs - one for each memory access port
- Clock enable for output registers
- Drop-in modules for the XC4000E, EX, XL, XV and Spartan families
- High performance and density guaranteed through Relational Placed Macro (RPM) mapping and placement technology
- Available in Xilinx CORE Generator

Functional Description

The dual-port RAM module has two independent memory access ports which permit shared access to a central pool of SelectRAM™. One port provides read/write access, the other read-only. Data can be read from the memory locations identified by the address, **A**, and dual-port address, **DPRA**, inputs by asserting clock enable **CE** and providing a rising edge on the clock input **C**. The contents of the memory location selected by the **A** input port is registered at the single-port output, **SPO**. The contents of the memory location selected by the **DPRA** input port is registered at the dual-port output, **DPO**. Note that neither **SPO** nor **DPO** change their values on rising clock edges where **CE** is low.

Data presented at the **D** input port may be stored at the memory location selected by the **A** address input, by asserting the write-enable input **WE** and providing a rising-edge on the clock input, **C**. Note that the contents of the memory location selected by the **A** address input remain unchanged on rising clock edges where **WE** is low.

The initial contents of the memory (i.e. the data stored in the memory immediately after device configuration) may also be specified.

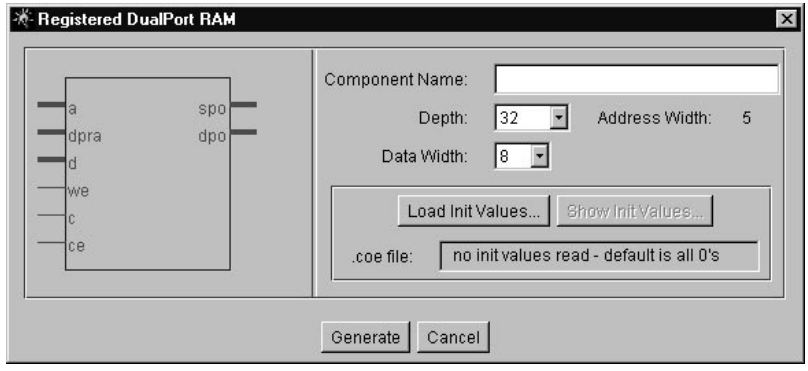

Figure 1: Parametrization Window

Pinout

Port names for the schematic symbol are show in Figure 2 and described in Table 1.

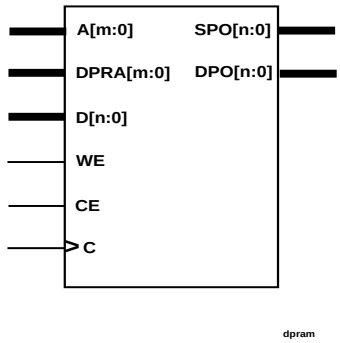

Figure 2: Core Schematic Symbol

Core Generator Parameters

The CORE Generator parameterization window for this module is shown in Figure 1. The parameters are as follows:

- **Component Name**: Enter a name for the output files generated for this module
- **Depth**: Select the number of words in the RAM from the pull-down menu. The number must be a multiple of 16 and within a range of 16 to 250.
- **Address Width**: The number of bits needed to address all of the words in the RAM. This is a read-only filed whose value is calculated form the value entered for depth.
- **Data Width**: Select an input bit width from the pull-down menu. The valid range is 2-31.
- **Load Init**: Values: Specifies the file that contains the initial values for each address.
- **Show Init**: Values: Displays the initial values after they have been loaded.
- **coe file**: Displays the name of the coefficient file. This is a read-only field.

Specifying Memory Contents

The initial contents of the Dual Port RAM memory can be assigned by specifying the desired information in a text file - known as a COE file. In addition to the initial memory contents, all the parameters visible on the parameterization window may be assigned values in the COE file. COE files may take any root filename but must end with the extension ".COE".

Table 1: Core Signal PInout

Signal	Signal Direction	Description
D[n:0]	Input	DATA IN - Data to be written into memory location selected by A input port when WE is active
A[m:0]	Input	ADDRESS - Memory address to which to write data from D input port when WE is active. Memory address from which to fetch data to register at the SPO output when CE is active.
DPRA[m:0]	Input	DUAL-PORT ADDRESS - Memory address from which to fetch data to register at the DPO output when CE is active.
WE	Input	WRITE ENABLE - When high, permits data to be stored in the memory. When low memory, contents are unchanged.
CE	Input	CLOCK ENABLE - When high data, from the selected memory addresses - selected by A and DPRA - is registered at the module's outputs SPO and DPO respectively. Outputs remain unchanged while CE is low.
C	Input	CLOCK - with the exception of asynchronous control inputs (where applicable), control and data inputs are captured, and new output data formed on rising clock transitions.
SPO	Output	DATA OUT - Data fetched from the memory address selected by the A input when CE is active.
DPO	Output	DUAL-PORT DATA - Data fetched from the memory address selected by the DPRA input when CE is active.

To select and load a COE file, press the “Load Init Values…” button on the parameterization window and choose the desired file from the dialog-box. To review the memory’s initial-values at any time, press the “Show Init Values…” button. Any field on the parameterization window that is assigned a value in the COE file will loose its previous value when the COE file is loaded. Changing a parameter value that was previously loaded from a COE file causes the COE file’s name to be highlighted in red, indicating that the settings have changed since the file was loaded.

For a detailed description of COE file syntax, please refer to the Xilinx CORE Generator User Guide. The list of COE file keywords supported by the Registered Dual Port RAM module are shown in the Parameter File Information table at the end of this datasheet. An example COE file is shown below.

When specifying the initial contents for a memory in a COE file, the keywords **DEFAULT**, **SIGNED** and **RADIX** may be used. The **DEFAULT** keyword allows a value to be assigned to all memory locations with a single, brief statement. The **DEFAULT** value is overridden for those memory locations for which **MEMDATA** is provided. When specifying **DEFAULT** or **MEMDATA** values, radix 10 is assumed. If values are expressed in hexadecimal, use the command **RADIX = 16** in your COE file. If **RADIX = 16**, **DEFAULT** and **MEMDATA** values must be positive and within the range 0 to $2^{DATA\_WIDTH\_1}$. If **RADIX** = 10, **DEFAULT** and **MEMDATA** values are assumed to be signed and must be within the range $-2^{(DATA\_WIDTH-1)}$ to $2^{(DATA\_WIDTH-1)}$. If however **RADIX** = 10 then you may add the command **SIGNED = FALSE** to your COE file. In this case **DEFAULT** and **MEMDATA** values must be positive and within the range of 0 to $2^{DATA\_WIDTH-1}$.

```
Component_Name=dprm48x8;
Data_Width=8;
Depth=48;
Radix=16;
MemData=0,1,2,3,4,5,6,7,8,9,
10,11,12,13,14,15,16,17,18,19,
20,21,22,23,24,25,26,27,28,29,
30,31,32,33,34,35,36,37,38,39,
40,41,42,43,44,45,46,47;
```

Figure 3: Example COE file for the Dual Port RAM

Core Resource Utilization

The number of CLBs required depends on the values of the depth and data width fields selected in the CORE Generator parameterization window.

Table 2 shows the equations to calculate the maximum number of CLBs required for selected depths and widths.

Table 2: Maximum Number of CLB’s

Depth	Data Width	CLB Count
16	N	N
32	N	3N
48	N	5N
>=64	N	(depth/16)(N+1)

Ordering Information

This macro comes free with the Xilinx CORE Generator. For additional information contact your local Xilinx sales representative, or e-mail requests to coregen@xilinx.com-Parameter File Information

Parameter File Information

Parameter Name	Type	Notes
Component_Name	String	
Data Width	Integer	2-31
Depth	Integer	16-256
Address_Width	Integer	4-8
MemData{n} 0<=n<=255	Integer	
Signed*	Boolean	True/False
Default*	Integer	
Radix*	Integer	10 or 16

*COE file only.