Registered ROM

July 17, 1998 Product Specification

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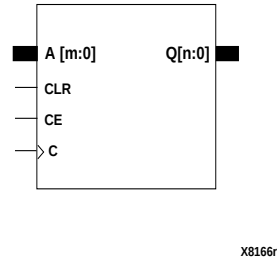

Figure 1: Core Schematic Symbol

Features

- Supported data width from 2 to 31 bits
- Supported depths from 16 to 256 words
- Registered output
- Clock Enable for output register
- Asynchronous clear of the output register
- Drop-in modules for the XC4000E, EX, XL, XV and Spartan families
- High performance and density guaranteed through Relational Placed Macro (RPM) mapping and placement technology
- Available in Xilinx CORE Generator

Functional Description

This macro creates a ROM whose size is determined by the data width and depth variables in the parameterization window. The output data is read from the ROM and registered. Data is read from the address selected or the A address pins. Access to the ROM is accomplished on the rising edge of the Clock signal when the CE pin is asserted (HIGH). A CLR signal can be used to clear the register asynchronously. The contents of the ROM are defined by creating a text file containing the desired information which is read during module parameterization.

Pinout

Signal names for the schematic symbol are shown in Figure 1 and described in Table 1.

CORE Generator Parameters

The core generator dialogue box for this macro is shown in Figure 2. The parameters are as follows:

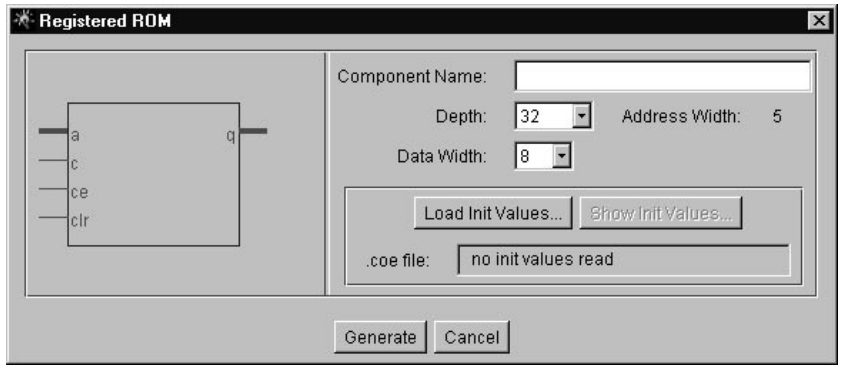

Figure 2: Parameterization Window

- **Component Name**: Enter a name for the output files generated for this module.
- **Depth**: Select the number of words in the ROM from the pull-down menu. The number must be a multiple of 16.
- **Address Width**: The number of bits needed to address all of the words in the ROM. This is a read-only field whose value is calculated from the value generated for depth.
- **Data Width**: Select an input bit width from the pull-down menu. The valid range is 2-31.
- **Load Init Values**: Specifies the file that contains the initial values for each address.
- **Show Init Values**: Display the initial values after they have been loaded.
- **coe file**: Displays the name of the coefficient file. This field is read-only.

Specifying Memory Contents

The contents of the Registered ROM module can be assigned by specifying the desired information in a text file - known as a COE file. In addition to the memory contents, all the parameters visible on the parameterization window may be assigned values in the COE file. COE files may take any root filename but must end with the extension ".COE".

To select and load a COE file, press the "Load Init Values…" button on the parameterization window and choose the desired file from the dialog-box. To review the memory contents at any time, press the "Show Init Values…" button. Any field on the parameterization window that is assigned a value in the COE file will loose its previous value when the COE file is loaded. Changing a parameter value that was previously loaded from a COE file causes the COE file's name to be highlighted in red, indicating that the settings have changed since the file was loaded.

For a detailed description of COE file syntax, please refer to the Xilinx CORE Generator User Guide. The list of COE file keywords supported by the Registered ROM module are shown in the Parameter File Information table at the end of this datasheet. An example COE file is shown below.

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
A [m:0]	Input	ROM ADDRESS – selects a particular ROM location.
CLR	Input	CLEAR – asynchronously resets the output register. Overrides the Clock and Clock Enable. Level sensitive.
CE	Input	CLOCK ENABLE – active high signal used to allow the transfer of data from ROM into the output register.
C	Input	CLOCK – with the exception of asynchronous control inputs (where applicable), control and data inputs are captured, and new output data formed on rising clock transitions.
Q[n:0]	Output	REGISTERED OUTPUT DATA – the registered output of the ROM.

When specifying the initial contents for a memory in a COE file, the keywords **DEFAULT**, **SIGNED** and **RADIX** may be used. The **DEFAULT** keyword allows a value to be assigned to all memory locations with a single, brief statement. The **DEFAULT** value is overridden for those memory locations for which **MEMDATA** is provided. When specifying **DEFAULT** or **MEMDATA** values, RADIX IO is assumed. If values are expressed in hexadecimal, use the command **RADIX = 16** in your COE file. If **RADIX = 16**, **DEFAULT** and **MEMDATA** values must be positive and within the range 0 to $2^{DATA\_WIDTH\_1}$. If **RADIX** = 10, **DEFAULT** and **MEMDATA** values are assumed to be signed and must be within the range $-2^{(DATA\_WIDTH-1)}$ to $2^{(DATA\_WIDTH-1)}$. If however **RADIX** = 10 then you may add the command **SIGNED = FALSE** to your COE file. In this case **DEFAULT** and **MEMDATA** values must be positive and within the range of 0 to $2^{DATA\_WIDTH-1}$.

```
Component_Name=rom48x8;
Data_Width=8;
Depth=48;
Radix=16;
MemData=0,1,2,3,4,5,6,7,8,9,
10,11,12,13,14,15,16,17,18,19,
20,21,22,23,24,25,26,27,28,29,
30,31,32,33,34,35,36,37,38,39,
40,41,42,43,44,45,46,47;
```

Figure 3: Example COE file for the Registered ROM

Core Resource Utilization

The number of CLBs required depends on the values of the depth and data width fields selected in the CORE Generator dialog box.

Table 2 shows the equations to calculate the maximum number of CLBs required for selected depths and data widths.

Table 2: Bit Width versus CLB Count

Depth	Data Width	CLB Count
16	2N	N
16	2N+1	N
32	N	N
48	N	2N
≥64	2N	(Depth/16) (N+1)
≥64	2N+1	(Depth/16) (N+1)

Ordering Information

This macro comes free with the Xilinx CORE Generator. For additional information contact your local Xilinx sales representative, or e-mail requests to coregen@xilinx.com.

Parameter File Information

Parameter Name	Type	Notes
Component_Name	String	
Data_Width	Integer	2 - 31
Depth	Integer	16 - 31
Address_Width	Integer	4 - 8
MemData{n} 0<=n<=255		
Signed*	Boolean	True/False
Default*	Integer	
RADIX*	Integer	10 or 16

*COE file only