Registered Single Port RAM

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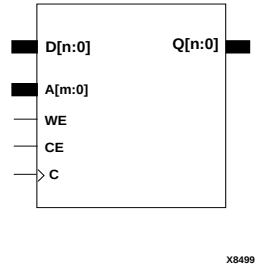

Figure 1: Core Schematic Symbol

Features

- Supports data widths from 2 to 31 bits
- Uses SelectRAM™ for more efficient storage
- Supports memory depths from 16 to 256 words
- Allows power-on memory content to be defined
- Registered output
- Clock Enable for output register
- Drop-in modules for the XC4000E, EX, XL, XV and Spartan families
- High performance and density guaranteed through Relational Placed Macro (RPM) mapping and placement technology
- Available in Xilinx CORE Generator

Functional Description

This module takes an N-bit data value and an M-bit address. During a write operation (rising edge on C with WE=1) the data value is stored in memory at the location selected by the address. (Note that if CE is also high, the previous contents of the selected memory location are registered at the module's outputs, Q.) During a read operation (rising edge on C with CE = 1) the contents of the memory location selected by the address are registered at the module's outputs.

The initial contents of the memory (i.e. the data stored in the memory immediately after device configuration) may also be specified.

Pinout

Port names for the schematic symbol are shown in Figure 1 and described in Table 1.

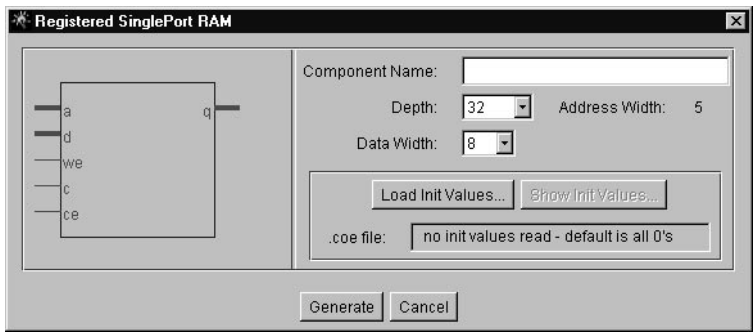

Figure 2: Parameterization Window

CORE Generator Parameters

The CORE Generator parameterization window for this macro is shown in Figure 2. The parameters are as follows:

- **Component Name**: Enter a name for the output files generated for this module.
- **Depth**: Select the number of words in the RAM from the pull-down menu. The number must be a multiple of 16 and within the range of 16 to 256.
- **Address Width**: The number of bits needed to address all of the words in the RAM. This is a read-only field whose value is calculated from the value entered for Depth.
- **Data Width**: Select an input bit width from the pull-down menu. The valid range is 2-31.
- **Load Init Values**: Specifies the file that contains the initial values for each address.
- **Show Init Values**: Display the initial values after they have been loaded.
- **coe file**: Displays the name of the coefficient file. This field is read-only.

Specifying Memory Contents

The initial contents of the Synchronous RAM memory can be assigned by specifying the desired information in a text file - known as a COE file. In addition to the initial memory contents, all the parameters visible on the parameterization window may be assigned values in the COE file. COE files may take any root filename but must end with the extension ".COE".

To select and load a COE file, press the "Load Init Values…" button on the parameterization window and choose the desired file from the dialog-box. To review the memory's initial-values at any time, press the "Show Init Values…" button. Any field on the parameterization window that is assigned a value in the COE file will loose its previous value when the COE file is loaded. Changing a parameter value that was previously loaded from a COE file causes the COE file's name to be highlighted in red, indicating that the settings have changed since the file was loaded.

For a detailed description of COE file syntax, please refer to the Xilinx CORE Generator User Guide. The list of COE file keywords supported by the Registered Synchronous RAM module are shown in the Parameter File Information table at the end of this datasheet. An example COE file is shown below.

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
D[n:0]	Input	DATA INPUT – data to be written into the RAM.
A[m:0]	Input	RAM ADDRESS – the memory location at which data will be stored (WE=1) or whose contents will be registered at the output (CE=1).
WE	Input	WRITE ENABLE – active high signal used to allow the transfer of data from the input data pins D[n:0] into the RAM.
CE	Input	CLOCK ENABLE – active high signal used to allow the transfer of data from the RAM into the output register.
C	Input	CLOCK – with the exception of asynchronous control inputs (where applicable), control and data inputs are captured, and new output data formed on rising clock transitions.
Q[n:0]	Output	REGISTERED OUTPUT DATA – the registered output of the RAM.

When specifying the initial contents for a memory in a COE file, the keywords **DEFAULT**, **SIGNED** and **RADIX** may be used. The **DEFAULT** keyword allows a value to be assigned to all memory locations with a single, brief statement. The **DEFAULT** value is overridden for those memory locations for which **MEMDATA** is provided. When specifying **DEFAULT** or **MEMDATA** values, radix 10 is assumed. If values are expressed in hexadecimal, use the command **RADIX = 16** in your COE file. If **RADIX** = 16, **DEFAULT** and **MEMDATA** values must be positive and within the range 0 to $2^{DATA\_WIDTH-1}$. If **RADIX** = 10, **DEFAULT** and **MEMDATA** values are assumed to be signed and must be within the range $-2^{(DATA\_WIDTH-1)}$ to $2^{(DATA\_WIDTH-1)}$. If however **RADIX** = 10 then you may add the command **SIGNED = FALSE** to your COE file. In this case **DEFAULT** and **MEMDATA** values must be positive and within the range of 0 to $2^{DATA\_WIDTH-1}$.

```
Component_Name=sram48x8;
Data_Width=8;
Depth=48;
Radix=16;
MemData=0,1,2,3,4,5,6,7,8,9,
10,11,12,13,14,15,16,17,18,19,
20,21,22,23,24,25,26,27,28,29,
30,31,32,33,34,35,36,37,38,39,
40,41,42,43,44,45,46,47;
```

Figure 3: Example COE file for the Synchronous RAM.

Core Resource Utilization

The number of CLBs required depends on the values of the depth and data width fields selected in the CORE Generator dialog box.

Table 2 shows the equations to calculate the maximum number of CLBs required for selected depths and data widths.

Table 2: Bit Width versus CLB Count

Depth	Data Width	CLB Count
16	2N	N
16	2N+1	N
32	N	N
48	N	2N+1
≥ 64	2N	(Depth/16) (N+1)
≥ 64	2N+1	(Depth/16) (N+2)

Table 3 shows the resource utilization for sample depths and bit widths.

Ordering Information

This macro comes free with the Xilinx CORE Generator. For additional information contact your local Xilinx sales representative, or e-mail requests to coregen@xilinx.com.

Table 3: Synchronous Single Port RAM Characterization Data

Depth	Data Width	CLB Count	Area Required for RPM (Rows, Columns)	4000XL-08 (Advanced) MHz	4000XL-09 MHz	4000XL-3 MHz	Spartan-4 (Advanced) MHz
16	4	2	2,1		192	136	142
16	8	4	4,1		151	105	141
16	16	8	8,1		132	93	140
16	24	12	12,1		125	88	125
32	4	4	4,1		148	111	142
32	8	8	8,1		135	96	123
32	16	16	16,1		123	86	110
32	24	24	24,1		115	79	
64	4	12	3,4		123	89	113
64	8	20	5,4		115	80	113
64	16	36	9,4				
64	24	52	13,4		106	73	95
128	4	24	3,8				
128	8	40	5,8				
128	16	72	9,8				
128	24	104	13,8				
256	4	48	3,16		90	63	83
256	8	80	5,16		83	57	58
256	16	144	9,16		77	51	36
256	24	208	13,16		70	48	23

Note: 1. To achieve the performance documented in this table, it may be necessary to specify a TIMESPEC (timing specification) PERIOD constraint appropriate to meet the documented frequency.
2. For some parameter combinations, the core is not 100% relationally placed. Therefore, the core's performance in your application may vary.

Parameter File Information

Parameter Name	Type	Notes
Component_Name	String	
Data_Width	Integer	2 - 31
Depth	Integer	16 - 256
Address_Width	Integer	4-8
MemData{n} 0<=n<=255	Integer	
Signed*	Boolean	True/False
Default*	Integer	
Radix*	Integer	10 or 16

*COE file only.