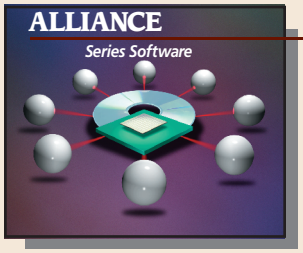

XILINX®

A2.1i CPLD Design Implementation Flow

Static Timing Analysis

vm6 → Timing Analyzer → tim, mod, data

Graphical Constraints Editor

ngd → Graphical Constraints Editor ↔ ucf

Timing Simulation

vm6 → tsim ngd2vhdl ngd2ver ngd2edif → vhd, v, edn, sdf

Simulation Options → tsim ngd2vhdl ngd2ver ngd2edif

sedif, sxnf, edif, edn, edf, xnf, pld, ncf → NGDBuild

ucf, ncf → NGDBuild

NGDBuild → ngd → FITTER → vm6, gyd

vm6 → BITSTREAM → jed

Pin Locking

gyd → PIN2UCF → ucf

JTAG Programmer

jed → JTAG Programmer

Main Flow

Options

EddieG99

PN 0010424 01

A2.1i CPLD Design Implementation Guide

Device Architecture Support

CPLD Product Family
XC9500

Xilinx Contacts and Technical Support

World Wide Web:
http://www.xilinx.com

North America
1-800-255-7778
hotline@xilinx.com
United Kingdom
44 1932-820821
ukhelp@xilinx.com

France
33 1-3463-0100
frhelp@xilinx.com
Japan
81 3-3297-9163
jhotline@xilinx.com

Guide Overview

1 Invoke the Design Manager

PC Invoke Design Manager
UNIX xilinx

Load the Design
File→New Project→Enter Input Design

Implement the Design
Design→Implement→Select target device, family, package, speedgrade.
Select "options" in Implement window Edit, Implementation and Timing Simulation templates. Select RUN to implement the design.

Guide Overview, Continued

2 Utilities and Tools

Utilities→Report Browser
Browse the report of the various Implementation process

Tools→Timing Analyzer
Perform a timing analysis on a design using available timing constraints

Utilities→Graphical Constraints Editor
Enter the Timing Constraints and I/O pin locations in Graphical Constraints Editor after the **Translate(ngdbuild)** process.

To Lock Pins
Implement Design, Select an implemented revision and Select Design→LockPins and generate pin locking constraints in UCF file format.

3 CPLD Programming

Tools→JTAG Programmer
To program your design in jedec file format to CPLD. It also performs operations such as verify, erase, functional test, blank check, readback jedec, get device id, get device checksum, get device signature/usercode, and bypass.

Notes:
In the flow engine, to stop after a particular implementation process, Select Setup→stop after→select a process stage.Use the stamp option in the trce command to generate a STAMP Model file (.mod) and a STAMP data file (.data) for board level static timing analysis.
Please refer to the **Xilinx Synthesis and Simulation Design Guide** for other options and commands for command line users.