# LogiCORE™

## Non-Symmetric, 16-Deep Time Skew Buffer

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**XILINX®**

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## Features

- Drop-in modules for the XC4000E, EX, XL, XV and Spartan families
- Uses SelectRAM™ for high density performance
- Supports serial word lengths up to 16 bits
- Clock enable for internal registers
- High performance and density guaranteed through Relational Placed Macro (RPM) mapping and placement technology
- Available in Xilinx CORE Generator

## Functional Description

This macro accepts a serial data input on the SDI pin. This data is stored in a series of Serially Cascaded, 16-bit Synchronous RAM-based shift registers. Each RAM's output data is registered and presented on the Q pins of the Macro. Each register's Q pin is internally cascaded to the following RAM's Data Input. The 16-bit RAM-based shift register supports 1- to 16-bit wide data storage per stage. The RESET pin is used to control the Bit-Width of the serial-data to be stored via external control logic. See timing diagram.

The internal RAM is generated internally by a free-running, 4-bit counter (CNT04RE). The counter is controlled by the CE and RESET inputs both active high.

## Pinout

Port names for the schematic symbol are shown in Figure 1 and Table 2.
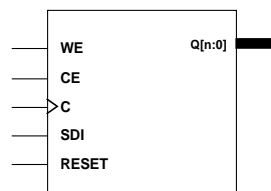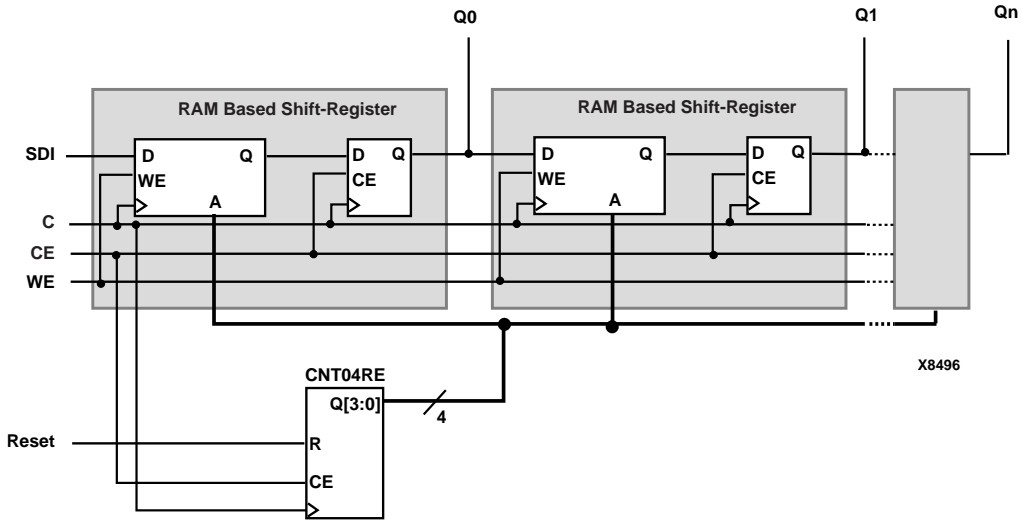


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**Figure 1: Core Schematic Diagram**
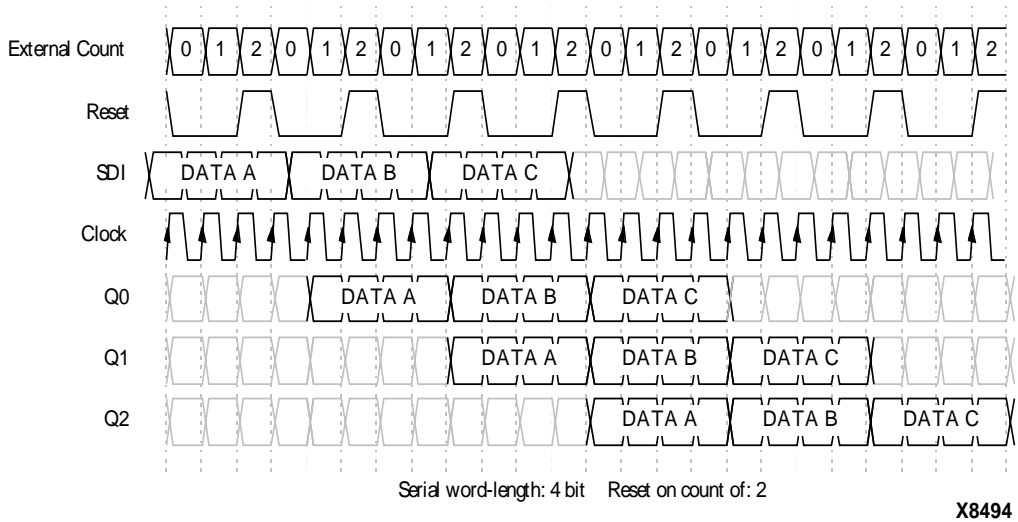
**Figure 2: Functional Block Diagram**



Serial word-length: 4 bit    Reset on count of: 2

X8494

**Figure 3: Timing Diagram: Example 3 delay states of 4-bit data.**

**Table 2: Core Signal Pinout**

| Signal | Signal Direction | Description |
|--------|------------------|-------------|
| WE | Input | WRITE ENABLE – Active high signal, Enables writing to the RAM in association with the internal address counter. |
| CE | Input | CLOCK ENABLE – active high signal used to allow the transfer of data from the internal RAM to the registered output and the incrementing of the internal Address counter. |
| C | Input | CLOCK – clocks the output registers, TSB Counter, and internal synchronous RAM. With the exception of asynchronous control inputs (where applicable), control and data inputs are captured, and new output data formed rising clock transitions. |
| SDI | Input | SERIAL DATA INPUT – data presented on this pin is stored into the TSB when the CE (CLOCK ENABLE) and WE (WRITE ENABLE) is asserted (HIGH) and the rising edge of the C (CLOCK). |
| RESET | Input | TERMINAL COUNT RESET – Used to reset the internal RAM's address counter to zero. RESET should be set high at a count of N-2 when storing N-bit data. |
| Q[N:0] | Output | REGISTERED OUTPUT DATA – the registered outputs of the RAMs. |

## Floorplan Information

This module is functionally identical to the "Non-symmetric 16-Deep Time Skew Buffer" but differ in terms of its floorplan or layout. This modules floorplan is derived as shown below:



X8520
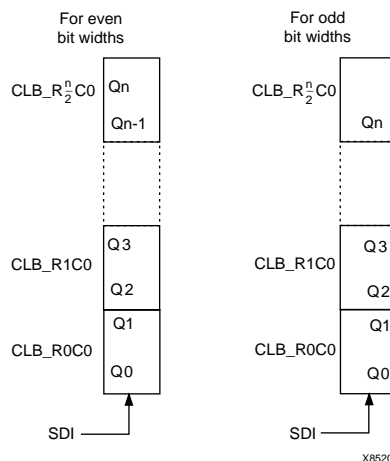
## CORE Generator Parameters

The CORE Generator parameterization window for this macro is shown in Figure 2. The parameters are as follows:

- **Component Name**: Enter a name for the output files generated for this module.
- **Output Width**: Select an input bit width from the pull-down menu. The valid range is 2-32.
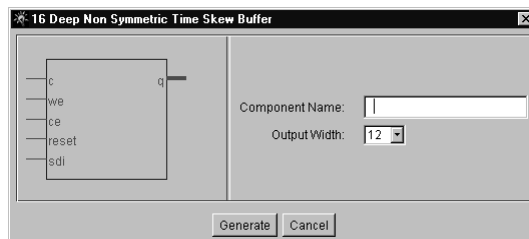


**Figure 4: Parameterization Window**

## Core Resource Utilization

Table 3 shows the number of CLBs required for each available bit width.

**Table 3: Bit Width versus CLB Count**

| Bit Width | CLB Count |
|---|---|
| 2 | 3 |
| 3 | 4 |
| 4 | 4 |
| 5 | 5 |
| 6 | 5 |
| 7 | 6 |
| 8 | 6 |
| 9 | 7 |
| 10 | 7 |
| 11 | 8 |
| 12 | 8 |
| 13 | 9 |
| 14 | 9 |
| 15 | 10 |
| 16 | 10 |
| 17 | 11 |
| 18 | 11 |
| 19 | 12 |
| 20 | 12 |
| 21 | 13 |
| 22 | 13 |
| 23 | 14 |
| 24 | 14 |
| 25 | 15 |
| 26 | 15 |
| 27 | 16 |
| 28 | 16 |
| 29 | 17 |
| 30 | 17 |
| 31 | 18 |
| 32 | 18 |

## Ordering Information

This macro comes free with the Xilinx CORE Generator. For additional information contact your local Xilinx sales representative, or e-mail requests to coregen@xilinx.com.

Parameter File Information

| Component Name | Type | Notes |
|---|---|---|
| Component_Name | String | |
| Output_Width | Integer | 2 - 32 |