LogiCORE™ Constant

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Xilinx Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
E-mail: corgen@xilinx.com
URL: www.xilinx.com

Features

- Drop-in modules for the XC4000E, EX, XL, XV and Spartan families
- Available in Xilinx CORE Generator

Functional Description

This module generates an object that forces a bus to a fixed value. The value may be expressed in any one of several useful formats.

Pinout

Port names for the schematic symbol are shown in Figure 1 and described in Table 1.

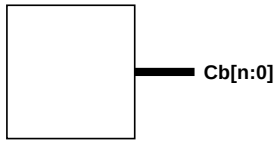

Figure 1: Core Schematic Symbol

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
Cb[n:0]	Output	CONSTANT – the fixed value applied to a bus.

CORE Generator Parameters

The CORE Generator parameterization window for this macro is shown in Figure 2. The parameters are as follows:

- **Component Name**: Enter a name for the output files generated for this module.
- **Output Width**: Select an input bit width from the pull-down menu. The valid range is 2-31.
- **Coefficient**: Enter the constant value.
- **Radix**: Select the radix: Hex or Decimal.
- **Sign**: If the radix is decimal, select the sign of the coefficient: Signed or Unsigned. If the radix is hex, the coefficient is always signed.

NEW SCREEN SHOT TO BE ENTERED

Figure 2: Parameterization Window

Core Resource Utilization

The constant is represented by a number of VCC GND primitives, so it does not use any resources.

Ordering Information

This macro comes free with the Xilinx CORE Generator. For additional information contact your local Xilinx sales representative, or e-mail requests to corgen@xilinx.com.

Parameter File Information

Parameter Name	Type	Notes
Component_Name	String	
Output_Width	Integer	2 - 31
Coefficient	Integer	