LogiCORE™

32-Word Deep Registered Look-Up Table

February 8, 1998 | Product Specification

XILINX®

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Features

- Drop-in modules for the XC4000E, EX, and XL families
- High performance and density guaranteed through Relational Placed Macro (RPM) mapping and placement technology
- Available in Xilinx CORE Generator

Functional Description

This macro is a registered look-up table, or ROM-based storage array. This is equivalent to an N-bit wide, 32-bit deep ROM. The address pins, A[4:0], are used to address the LUT data. The output of the LUT is registered on the rising edge of the C (CLOCK) signal with the CE (CLOCK ENABLE) signal asserted (HIGH).

The ROM data is defined via the INIT attributes. The INITs are attached to the LUT by the CORE Generator, which defines the memory's contents.

Pinout

Signal names for the schematic symbol are shown in Figure 1 and described in Table 1.

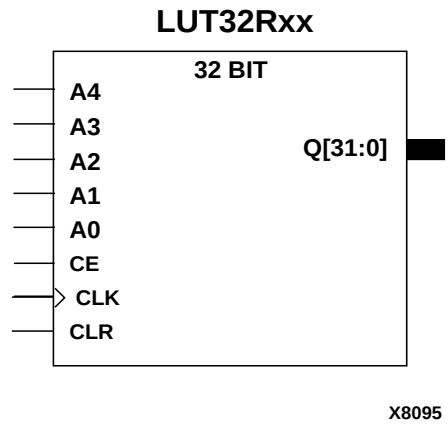

Figure 1: Core Schematic Symbol

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
A[4:0]	Input	ADDRESS – the ROM location, predefined by the INIT value, is decoded from these Address pins and presented to the register's input
CE	Input	CLOCK ENABLE – active high signal used to enable the transfer of data from the LUT to the output register
CLK	Input	CLOCK – clocks the output register on the rising edge
CLR	Input	ASYNCHRONOUS CLEAR – clears the register. Does not require the Clock or CE signal
Q[N-1, 0]	Output	REGISTER LUT DATA OUTPUT – the registered output of the look-up table

CORE Generator Parameters

The CORE Generator dialog box for this macro is shown in Figure 2. The parameters are as follows:

- **Component Name**: Enter a name for the output files generated for this module.
- **Data Width**: Select an input bit width from the pull-down menu. The valid range is 2-31.
- **LUT Data**: Enter the data for each address location.
- **Radix**: Select the radix of the LUT data: Hexadecimal or Decimal.
- **Sign**: If the radix is decimal, select the sign of the constant value: Signed or Unsigned. If the radix is hex, the constant is always signed.
- **Read From File**: In the pop-up window, set the name of the file that contains your LUT data.

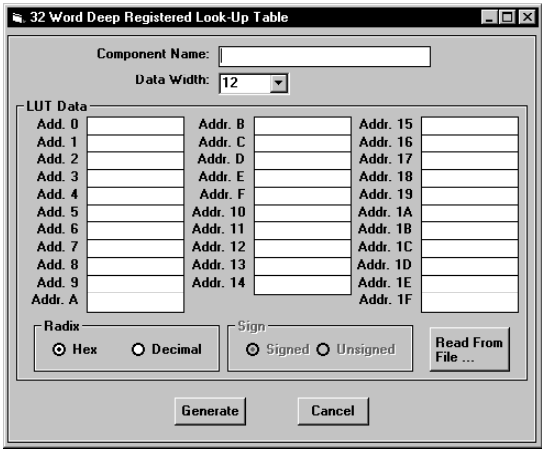

Figure 2: CORE Generator Dialog Box

Core Resource Utilization

Table 2 shows the number of CLBs required for each available bit width.

Ordering Information

This macro comes free with the Xilinx CORE Generator. For additional information contact your local Xilinx sales representative, or e-mail requests to dsp@xilinx.com.

Table 2: Bit Width versus CLB Count

Bit Width	CLB Count
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
10	10
11	11
12	12
13	13
14	14
15	15
16	16
17	17
18	18
19	19
20	20
21	21
22	22
23	23
24	24
25	25
26	26
27	27
28	28
29	29
30	30
31	31
32	32