M8259 Programmable Interrupt Controller

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Product Specification

Virtual IP Group, Inc.

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Features

- Eight Level Priority Controller
- Expandable to 64 Levels
- Programmable Interrupt Mode
- Individual Request Mask capability

Applications

Applications that require Programmable Interrupt Mode of operation for multiple interrupts.

General Description

The M8259 is a programmable interrupt controller core is used in most microcontroller/microprocessor systems to control and prioritize interrupts. It can handle up to 8 interrupt with programmable masking and priority for the interrupts. It can also be cascaded with up to 8 more M8259 blocks to handle more than 8 interrupts without any additional logic circuits. This design is functionally compatible with Intel's 8259 part.

AllianceCORE™ Facts

Core Specifics		
Device Family	Spartan	XC4000E
CLBs Used	191	191
IOBs Used	26[1]	26[1]
System Clock f_{max}	7.5 MHz	7.5 MHz
Device Features Used	Global Buffers	
Supported Devices/Resources Remaining		
	I/O	**CLBs**
XCS40PQ240-3	167[1]	593
XC4020EHQ240-2	167[1]	593
Provided with Core		
Documentation	Core Design Document Designer's Application Note FPGA Design Document	
Design File Formats	.ngd, XNF netlist Verilog Source RTL	
Constraint Files	.cst file, xactinit.dat	
Schematic Symbols	None	
Verification Tool	Test Vectors	
Evaluation Model	None	
Reference designs & application notes	FPGA Design Document included	
Additional Items	None	
Design Tool Requirements		
Xilinx Core Tools	Alliance 1.3	
Entry/Verification Tool	Verilog RTL/Verilog XL simulator	
Support		
Support provided by Virtual IP Group, Inc.		

Notes:
1. Assuming all core signals are routed off-chip.

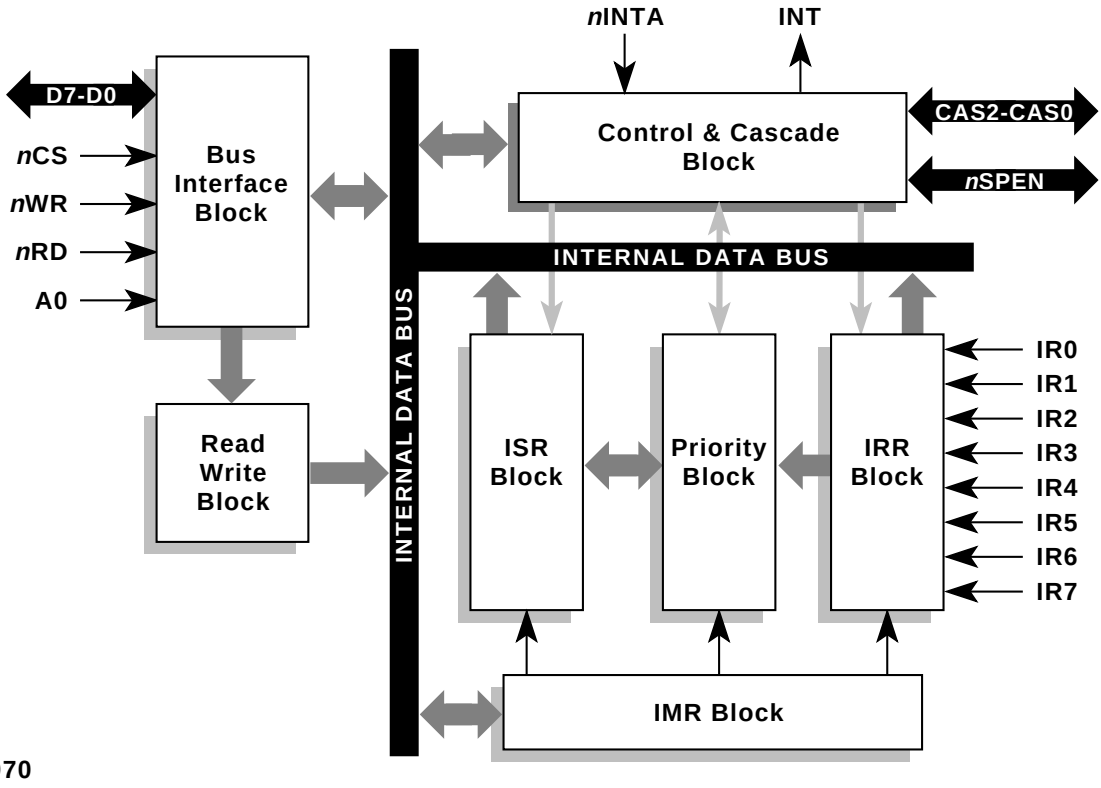

Figure 1: M8259 Functional Block Diagram

Functional Description

The M8259 core is partitioned into modules as shown in Figure 1 and described below.

Bus Interface Block

This block interfaces the core to the system bus. It also generates the internal read, write signals for the read/write block of the core.

Read/Write Block

The read / write block generates various read and write signals for reading status and writing command words.

Interrupt Mask Register (IMR) Block

This block is used for masking the interrupt inputs and masking the ISR bits in the special mask mode.

Interrupt Request Register (IRR) Block

This block stores all interrupt levels that are requesting service.

Interrupt Service Register (ISR) Block

The main function of this block is to store interrupt levels that are being serviced.

Priority Block

This block resolves the priority of valid interrupt request inputs and generates an encoded interrupt request for the control block of the core.

Control Block

This block controls the entire function of core and generates the external interrupt output signal.

Core Modifications

Multiple cores can be cascaded to build support for more Interrupts.

Pinout

The pinout has not been fixed to specific FPGA I/O allowing flexibility with the users application. However for the evaluation board, a pinout has been fixed. This information is provided in the FPGA Design Documentation. Signal names are provided in the block diagram shown in Figure 1 and Table 1.

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
Bus Interface Signals		
D[7:0]	In/Out	8 bit bidirectional CPU data bus through which CPU reads from or writes into core
NCS	Input	Active low chip select signal
NWR	Input	Active low write signal
NRD	Input	Active low read signal
A0	Input	Address signal for selection of internal registers
Control and Cascade Signals		
NINTA	Input	When active low, interrupt acknowledge signal is asserted, core drives programmed interrupt vector onto data bus
INT	Output	Interrupt output signal.
CAS [2:0]	In/Out	Cascade lines used to cascade up to 8 Interrupt controllers for a total capacity of 64 interrupts
NSPEN	Input	Slave program/enable; indicates master/slave mode operation for M8259 in non-buffered mode
IRR Signals		
IR [7:0]	Input	Input interrupt requests for core

Verification Methods

The core has been tested with in-house developed test vectors that are provided with the core. It has also been tested in the FPGA using a hardware evaluation board.

Recommended Design Experience

Knowledge of interface in Microprocessor based systems is required. The user must be familiar with HDL design methodology as well as instantiation of Xilinx netlists in a hierarchical design environment. Experience in usage of Alliance or Foundation tools is required.

Available Support Products

FPGA Evaluation Board

The FPGA Design Document included with the core gives directions for constructing a general purpose FPGA evaluation daughter board that can be plugged into a standard part socket on the target system through a flat cable.

Simulation Model

In-house developed test vectors are provided to test complete functionality and interface of the core.

Ordering Information

This product is available from Virtual IP Group, Inc. Please contact them for pricing and additional information.

Related Information

The user should refer to the Specification Document for programming this core for a typical application in a system. The user should also refer to the Designer's application note for integrating this with other cores.

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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