Spartan ä-II Family FAQ

1. What is the Spartan-II family?
   The Spartan-II family is the next generation family of the Spartan Series based on the industry-leading Virtex architecture. The Spartan-II family extends the portion of the ASIC market that Xilinx can address, while leveraging off the features and performance of the Virtex architecture. In addition, the increase in density, performance, and the availability of a broad base of cores, strongly positions the Spartan-II family as an ASSP (Application Specific Standard Products) replacement FPGA by integrating several features on-chip that would otherwise be found in discrete ASSP devices. The Spartan-II family is a 0.18u/0.22u, 2.5V family offering five devices in densities up to 150,000 system gates.

2. What are the differences between the Spartan-II family and Spartan-XL family?
   The Spartan-II family is:
   - Based on a cost-optimized Virtex architecture, while the Spartan-XL family is based on the XC4000 architecture
   - Based on a 0.18u/0.22u, six layer metal (6LM) process vs. a 0.25u/0.35u, five layer metal (5LM) process for the Spartan-XL family
   - >3x density increase (from 40,000 to 150,000 system gates)
   - >1.5x speed grade performance (from 100MHz to 150+MHz)
   - 2-3x gates per I/O pin
   - 2x gates per dollar
   - 2x I/O performance
   - Integrates more ASSP system functions, such as PLL clocks, FIFO memories, translators, and bus interfaces (PCI)
   - Operating voltage of 2.5V vs. 3.3V for the Spartan-XL family
   - Features an enhanced power-down with register preserve and status pin
   - Features dedicated BlockRAM in addition to SelectRAM, while the Spartan-XL family only has SelectRAM
   - Features dedicated DLLs for advanced clock control, while the Spartan-XL family does not
   - Available in fine pitch packages (FG256 and FG456)

3. What process technology is the Spartan-II family designed in?
   The Spartan-II family is designed in a 0.18u/0.22u, 6LM advanced process technology providing cost optimization and higher performance while remaining 5V tolerant. The Spartan-II family combines 0.22u transistors to maintain 5V compatibility, with 0.18u interconnect to reduce overall die size and provide higher speed.

4. What are some of the new markets and applications that the Spartan-II family will target for penetration?
   The Spartan-II family will be targeted for similar application markets that the Spartan and Spartan-XL family are currently found in, such as low-cost networking Small Office/Home Office (SOHO) equipment, telecommunications line cards, digital modems, video capture & editing equipment, cell phones, printers, and set-top boxes. The target market for the Spartan-II family is an ASIC, ASSP or FPGA user looking for a production solution at $10 or less in high volumes. With these revolutionary price points and higher density offerings, the Spartan-II family of FPGAs will be able to further penetrate non-traditional, high volume markets previously held by ASICs. Spartan-II FPGAs will serve as an ASSP replacement for high volume applications in the consumer, PC-related and communication markets. In addition, the Spartan-II family will continue to address the traditional strong FPGA markets: networking, telecommunications, high-end computing, industrial and wireless markets. These applications include switches, routers, line cards, and DSL modems.

5. Are Spartan-II FPGAs pin-to-pin compatible to prior Spartan Series product offerings?
   No, the Spartan-II FPGA is based on a cost-optimized Virtex architecture and is neither pin-to-pin nor software compatible with prior Spartan Series product offerings, which was based on the XC4000 architecture.

6. Is the new Spartan-II family footprint compatible with the Virtex family devices?
   No, Spartan-II family has different features and different package offerings from that of the Virtex family.

7. What are the differences between the Spartan-II family and the Virtex family since the two are based on the same architectures?
   Spartan-II FPGAs are a cost-optimized Virtex architecture designed in a 0.18u/0.22u, 6LM process, while Virtex FPGAs are currently in the 0.22u, 6LM process. In the first half of 2000, Virtex FPGAs will also be available in the 0.18u/0.22, 6LM process. From a price standpoint, the Spartan-II family will feature more aggressive high volume pricing than the Virtex family. From a feature standpoint, Spartan-II FPGAs are the same as Virtex FPGAs with the exception of the low power features. Spartan-II FPGAs have replaced the two temperature diode pins found on Virtex FPGAs with two pins for low power (powerdown and powerdown status). The Spartan-II family will be available in only the most popular and lowest cost package parts, which results in lower prices to our customers.

8. What are the architectural differences between the Spartan-II, Spartan-XL and Spartan families of FPGAs?

The Spartan-II family is based on the Virtex family architecture, while the Spartan and Spartan-XL family are based on the XC4000 Series architecture. The 2.5V Spartan-II devices are a cost-optimized Virtex architecture combining 0.22u transistors for 5V compatibility with 0.18u interconnect. The 5V Spartan devices combine 0.5u transistors, required for the 5V supply, with 0.35u interconnect. Meanwhile, the 3.3V Spartan-XL devices have 0.35u transistors, with a special I/O design for 100% 5V I/O compatibility, and 0.25u interconnect. While the Spartan and Spartan-XL families are footprint compatible with common packages within the series, the Spartan-II family is not footprint compatible with the prior Spartan Series members.

9. How will the availability of the Spartan-II family affect the Virtex family?
   Although Spartan-II FPGAs and Virtex FPGAs are based on the same architecture and there are only two packages that are common between the two families (FG256 and FG456). Xilinx does not foresee many customers switching from the Virtex family to the Spartan-II family even though Spartan-II FPGAs will be lower cost devices. This is because the overall costs of design migration over from the Virtex family to the Spartan-II family will not provide a substantial cost savings unless the application is targeted for high volumes.

10. What software supports the Spartan-II family?
    The Spartan-II family software support is available today. Xilinx and other EDA vendors, including Exemplar, Synopsys and Synplicity offer support via VHDL and Verilog synthesis. The latest software release, version of 2.1i of Xilinx Alliance Series and Foundation Series software, offer full support for the Spartan-II family.

11. What are the available packages?
    The Spartan Series product line philosophy has been to provide only the most popular and lowest cost package parts, which results in lower prices for our customers. The Spartan-II family continues this tradition with package offerings of VQ100, PQ208, CS144, TQ144, FG256 and FG456.

Package	2S15	2S30	2S50	2S100	2S150
VQ100	✓	✓			
CS144	✓	✓			
TQ144	✓	✓	✓	✓	
PQ208		✓	✓	✓	✓
FG256			✓	✓	✓
FG456				✓	✓

12. What are the devices in the family?

Device		2S15	2S30	2S50	2S100	2S150
Logic Cells		432	972	1728	2700	3888
Block RAM Bits		16,384	24,576	32,768	40,960	49,152
Max. User I/Os		82	128	176	196	260
Packages	14X14	VQ100	VQ100			
	12X12	CS144	CS144			
	20X20	TQ144	TQ144	TQ144	TQ144	
	28X28		PQ208	PQ208	PQ208	PQ208
	17X17			FG256	FG256	FG256
	23X23				FG456	FG456

13. What operating voltage will the Spartan-II family perform to?
    The Spartan-II family will run at 2.5V operating voltage and is designed for 3.3V and 5V I/O compatibility.

14. How will the additional performance and system features found in the Spartan-II family benefit the customer?
    The additional performance and system features in the Spartan-II family (such as the synchronous BlockRAM, DLLs, and Select I/O) will allow the user to achieve a higher level of system integration, thereby reducing overall system power requirements, and providing lower BOM costs and board space savings. This will also dramatically increase the number of system gates that can be integrated into a Spartan-II device, taking advantage of our higher number of gates per dollar.

15. What routing advantages does the Virtex architecture provide for the Spartan-II family?
    The much richer routing resources and the basic Virtex architecture will result in very fast compile times (on the order of 100,000 gates per minute) for the Spartan-II family with high performance results as well. This will enable the Spartan-II family to produce very predictable results in a short time for HDL users.

16. Will the Spartan-II family have the capability to support Internet Reconfigurable Logic (IRL)?
    Yes, the Spartan-II family will incorporate the configuration features of the Virtex Series (including partial reconfiguration) that support our Xilinx On-Line campaign and the concept of Internet Reconfigurable Logic. For more information, go to http://www.xilinx.com/xilinxonline/

17. What are the key points to remember about the Spartan-II family?
    - New features and higher performance than the Spartan-XL family
    - Software and cores before silicon
    - 100,000 gates for $10

- Reprogrammability at ASIC prices
- True ASSP replacement FPGA
- The Spartan-II family uses professional tools to deliver designs quickly

18. How will the launching of the Spartan-II family affect the launching of Virtex-E family?
    The Spartan-II family extends the portion of the ASIC market that the Spartan Series can address. The Spartan-II family will also serve as an ASSP replacement FPGA featuring low cost and low power, targeting the non-traditional, high volume application markets. The Virtex-E family showcases new features and performance, which target application markets that require the next level of performance, density and system integration from FPGAs.

19. Are the Spartan-II devices bitstream compatible with the Virtex devices?
    Although the Spartan-II devices are based on the Virtex architecture, Xilinx does not guarantee that the Spartan-II devices will be 100% bitstream compatible with Virtex devices.

20. What are the available cores for the Spartan-II family?
    The Spartan-II devices will be able to utilize the available cores from the Virtex devices that share the common densities between the two families (50K, 100K, and 150K system gates.) Today, there are 30 cores released for the Spartan-II family, which include PCI, Reed Solomon Decoder, Viterbi Decoder, etc. In addition, Xilinx is working with the Alliance Cores partners to develop new cores for the Spartan-II family as well as our own Xilinx LogiCores.

21. What various temperature grades will be available for the Spartan-II family?
    The Spartan-II family will be available in temperature grades of commercial and industrial for selected density and packages.

22. Is the speed naming convention the same for the Spartan-II family as it was for the Spartan and Spartan-XL family?
    Yes, the higher the number, the faster the device is. For example, the XC2S150-6 is faster than the XC2S150-5.

23. What advantages does the Spartan-II family serve as an ASSP replacement FPGA?
    With the built-in features of the Spartan-II family, this will eliminate the need for components such as phase lock loops, voltage translation buffers, and memory when on-chip RAM is sufficient. This high level of integration allows designers to reduce overall system power requirements, cut costs, and save board space making the Spartan-II family the low-cost, board level center for system design.