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FOR IMMEDIATE RELEASE

XILINX ANNOUNCES SUPPORT FOR TWO-MILLION-GATE FPGAS

Xilinx Alliance Series software delivers industry's fastest compile times and first Internet Team Design methodology

SAN JOSE, Calif., May 17, 1999—Xilinx Inc., (NASDAQ:XLNX) today announced its new Alliance Series version 2.1i software. Version 2.1i software delivers 50 percent reduction in compile times over the previous version, v1.5i software. This continues the trend that Xilinx has established during the last few years of reducing compile times for a given design size by 50 percent with each release. This new version also delivers advanced methodologies that support the design of the industry's first two-million-gate Virtex FPGAs, with these devices available later this year. Demonstrations of Alliance Series version 2.1i software will be given at the Design Automation Conference in Xilinx booth #2532.

"The designs that are being implemented in programmable logic today are more complex and are representing the most strategic aspects of our customers systems, said Rich Sevcik, Xilinx senior vice president of software, cores and support. "Our Internet Team Design (ITD) capabilities allow customers to implement designs and share IP across design teams and geographies, which is paramount in designing systems-based programmable logic."

Along with the runtime improvements and increased clock speeds, this release includes the new Xilinx Internet Team Design (ITD) methodology allowing teams of designers around the world to collaborate on multi-million gate designs via the Internet. Other productivity enhancing features of the v2.1i release are the new CORE Generator interface, improved floorplanning, data sheet-style timing reports, and a hierarchical browser for doing comprehensive post-layout timing analysis.

Two-Million-Gate Support

The next generation of place and route capability from Xilinx results in a significant reduction in placement times for Virtex-based architectures. This dramatically increases designer productivity as it enables many design iterations each day—even when designing with the two million plus system gate Virtex devices.

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"As device densities reach two-million gates, we remain focused on decreasing compile times," said Sevcik. “At the push of a button, designers can now compile the 100,000 system gate Virtex device in less than one minute. And, given the broad suite of cores supporting Virtex FPGAs today, high-level systems functions including the a 64 bit/66 MHz PCI interface can be implemented in less than 20 minutes."

Through close collaboration with our Alliance EDA partners, synthesis is now optimized for Virtex FPGAs. The ability to infer within synthesis the architectural features such as delay locked loops (DLL) and block RAM provides a more simplified design entry method while improving utilization. This feature coupled with fast compile times enables the productivity necessary to accomplish multiple design turns per day to meet the challenge of decreasing time to market.

Proper board-level verification becomes critical when designing systems with multi-million gate high-performance Virtex parts. Version 2.1i software delivers effective integration into board-level static timing analysis tools—a requirement for these types of designs. Xilinx now provides STAMP models with both minimum and maximum delay timing information for use with Mentor and Viewlogic board-level static timing. For system-level simulation, Synopsys supports Xilinx with its Logic Modeling SmartModels family.

Pioneering Internet Team Design (ITD) methods

Continuing in the Silicon Xpresso initiative and leveraging the current functionality of the Internet, Xilinx has enabled ITD capabilities within this version of Alliance Series software. The ITD tool is an innovative new way to meet the challenges of building complex, mega-gate designs by allowing teams of designers to build high-density programmable logic designs over the Internet. This add-on product will be available for purchase over the Web.

As Xilinx device densities approach two million system gates and beyond, designers must coordinate multiple design modules from others in remote locations. The ITD tools use the Internet to deliver improved communication between all members of the design team; to coordinate the different design source files; and to expertly integrate different design flows seen in today's typical FPGA design.

The ITD method creates a designer website that resides on the users' internal network. This website is a forms-based Web page where designers log-on and submit their design files to the project using their chosen Internet browser. Once submitted, the files are merged into a design project using ITD's Design Control System (DCS). The DCS behaves as a Web-based revision management system

that insures that the various iterations of a design's modules are properly linked into the top-level design. Using the ITD tool, the design team leader can easily integrate the design modules and place-and-route the design using the standard Xilinx implementation tools included within the Xilinx Alliance Series software. Once the design is placed and routed, detailed reports are issued to the ITD website for review by the design team. In this way, the team can brainstorm and collaborate on the creation of any additional iterations.

About Alliance Series software

The Alliance Series 2.1i software provides architecture-specific device support for all Xilinx product families, including Spartan/XL, Virtex, XC4000X, XC4000XV, XC3100A/L, and XC5200 FPGAs, plus XC9000 CPLDs. The new software will be available in June for popular PC and workstation platforms and operating systems such as Windows95 and Windows NT; Chinese, Korean, and Japanese Windows; Solaris and HP-UX. The new Alliance Series software pricing starts at $95. Evaluation software is also available for qualified users.

Xilinx is the leading innovator of complete programmable logic solutions, including advanced integrated circuits, software design tools, predefined system functions delivered as cores, and unparalleled field engineering support. Founded in 1984 and headquarters in San Jose, Calif., Xilinx invented field programmable gate arrays (FPGA) and commands more than half of the world market for these devices today. Xilinx solutions enable customers to significantly reduce the time required to develop products for the computer, peripheral, telecommunication, networking, industrial control, instrumentation, high-reliability/military, and consumer markets. For more information, visit the Xilinx web site at www.xilinx.com.

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